Pixel Detectors for Charged Particles

N. Wermes
Bonn University
Pixel detectors for charged particle tracking/vertexing

Hybrid Pixel Detectors

⇒ all large detectors (i.e. LHC) so far

(Semi)-Monolithic Pixel Detectors

⇒ most new developments except for sLHC
MAPS (epi), MAPS (SOI), DEPFET, 3D-integration
The “PAST”: large area pixel detectors at the LHC

all based on

“Hybrid Pixel Detectors”
Principle of hybrid pixel detector readout

charge generation in sensor, integration in FE-chip

temporary on chip storage (digital or analog) 
trigger driven readout of individual hits

- pn-diode $\Rightarrow Q_{signal}$
- amplification and filtering $\Rightarrow V_{out}$
- pixel-wise storage: address, charge, time (BX)
- column-wise R/O
- transfer information to End of Column (wait for trigger)
Principle of hybrid pixel detector readout

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temporary on chip storage (digital or analog)
trigger driven readout of individual hits

- \( q \rightarrow Q_{\text{signal}} \)
- amplification and filtering \( \rightarrow V_{\text{out}} \)
- pixel-wise storage: address, charge, time (BX)
- column-wise R/O
- transfer information to End of Column (wait for trigger)

✓ high rate capability
✓ radiation hard to \( 10^{15} \) \( n_{eq}/cm^2 \)
✓ mature technology

❖ comparatively massive (>3% \( X_0 \), mostly due to power and “overall size”)
❖ resolution \( \sim 10 \) \( \mu m \) (pixels sizes 50x400 \( \mu m^2 \) or 100x150 \( \mu m^2 \))
A Hybrid Pixel Detector Module

- module (1.1% $X_0$)
- supports & cables (2.4% $X_0$) per layer
Principle of (semi-) monolithic pixel detectors

generation and processing of signal in “same” substrate

- pn-diode $\Rightarrow Q_{\text{Signal}}$
- collection diode (transistor gate)
  $\Rightarrow U_{\text{Signal}} = Q_{\text{Signal}} / C_g$
  or $I_{\text{Signal}} = g_m \cdot Q_{\text{Signal}} / C_g$
- row wise selection of pixels
- column wise readout
- select/reset switch

CMOS active pixels
- same CMOS substrate
  for steering/readout electronics
  and for $Q$ – collection

DEPFET pixels
- one amplifying transistor on fully depleted bulk
  separate steering and R/O chips

at least so far …
Principle of (semi-) monolithic pixel detectors

generation and integration of signal in “same” substrate

- pn-diode \( \Rightarrow Q_{\text{Signal}} \)
- collection diode (transistor gate)
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- same CMOS substrate
  for steering/readout electronics
  and for \( Q \) – collection

DEPFET pixels
- one amplifying transistor on fully depleted bulk
  separate steering and R/O chips
Rate and radiation challenges at the innermost pixel layer

<table>
<thead>
<tr>
<th>Hybrid Pixels</th>
<th>Monolithic Pixels</th>
</tr>
</thead>
<tbody>
<tr>
<td>lower rates</td>
<td>smaller pixels</td>
</tr>
<tr>
<td></td>
<td>less material</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>BX time</th>
<th>Particle Rate</th>
<th>Fluence</th>
<th>Ion. Dose</th>
</tr>
</thead>
<tbody>
<tr>
<td>ns</td>
<td>kHz/mm²</td>
<td>nₑq/cm² per lifetime*</td>
<td>kGy per lifetime*</td>
</tr>
<tr>
<td>LHC (10³⁴ cm⁻²s⁻¹)</td>
<td>25</td>
<td>1000</td>
<td>1.0 x 10¹⁵</td>
</tr>
<tr>
<td>superLHC (10³⁵ cm⁻²s⁻¹)</td>
<td>25</td>
<td>10000</td>
<td>10¹⁶</td>
</tr>
<tr>
<td>SuperBelle (10³⁵ cm⁻²s⁻¹)</td>
<td>2</td>
<td>400</td>
<td>~3 x 10¹²</td>
</tr>
<tr>
<td>ILC (10³⁴ cm⁻²s⁻¹)</td>
<td>350</td>
<td>250</td>
<td>10¹²</td>
</tr>
<tr>
<td>STAR@RHIC (8x10²⁷ cm⁻²s⁻¹)</td>
<td>110</td>
<td>3,8</td>
<td>1.5 x 10¹³</td>
</tr>
</tbody>
</table>

assumed lifetimes:
LHC, sLHC: 7 years
ILC: 10 years
others: 5 years

Hybrid Pixels

Lower rates
Small pixels
Less material

Monolithic Pixels
Pixels for super-LHC (2016)

current directions

note: intermediate step $\rightarrow$ B-layer upgrade/replacements scenarios (~2012)
Main issues @ sLHC

• radiation hardness

Radial distribution of sensors determined by Occupancy

- Long Strips (up to $4 \times 10^{14}$ cm$^{-2}$)
- Short Strips (up to $10^{15}$ cm$^{-2}$)
- Pixels (up to $10^{16}$ cm$^{-2}$)

sATLAS Fluences for 3000fb$^{-1}$

Fluence neq/cm$^2$

- All: RTF Formula
- $n$ (5cm poly)
- pion
- proton

Fluence: $10^{15} - 10^{16}$ cm$^{-2}$

Radiation hardness:
- ~$10^{16}$ n$_{eq}$/cm$^2$ at innermost layers
- New sensor R&D ongoing: 3D silicon, planar (n in p), diamond

Data rate:
- Output rate at innermost layer = 320 MHz = 4 x LHC

Material:
- Strong interplay between: resolution – secondaries – pattern/track algorithms

What is the best detector? More layers? Less material?

New powering concepts needed (serial, DC-DC)

Goal: 1.5 – 2% X$_0$ factor 2 reduction wrt LHC
Main issues @ sLHC

• **radiation hardness**
  – \( \sim 10^{16} \text{n_{eq}/cm}^2 \) @ innermost layers
  – new sensor R&D ongoing: 3D-silicon, planar (n in p), diamond

• **data rate**
  – output rate at innermost layer = 320 MHz = 4 x LHC

• **material**
  – strong interplay between: resolution – secondaries – pattern/track algorithms
    \( \Rightarrow \) what is the best detector? more layers? less material?
  – new powering concepts needed (serial, DC-DC)
  – goal: 1.5-2% \( X_0 \) \( \Rightarrow \) factor \( \sim 2 \) reduction wrt. LHC (!)
sLHC Sensor R&D

3D silicon

Technique: Deep Reactive Ion Etching (DRIE)

- shorter drift distance $\rightarrow$ fast
- lower voltages
- better radiation tolerance
- sensor edge can be an electrode

$\n$ inefficient in area of electrode
$\n$ manufacturing yield & costs $=$ ?

3D collaboration: C. da Via’, S. Parker, C. Kenney et al.
3D: test beam results (100 GeV $\pi$)

- Stanford devices, unirradiated
- pixel electronics (ATLAS FE-I3)

M. Mathes et al., IEEE TNS 2008 (accepted)

3E device = 3 electrodes/pix with ATLAS pixel geometry
columns reach through bulk

- $V_{\text{depl}} \sim 10$ V
- efficiency 95.6% ($0^\circ$ tracks)
  99.9% ($15^\circ$ tracks)
- spatial resolution as for planar pixels (~12 µm)
diamond (poly crystalline and single crystal)

✓ has finally become competitive (to Si)
  ✓ large band gap (x5) → no leakage current → no shot noise
  ✓ smaller $\varepsilon_r$ (x 0.5) → lower input capacitance → lower thermal and 1/f noise
  ✓ small $Z=6$ → large radiation length (x2 in g/cm$^2$)
  ✓ narrower landau distribution (by 10%)

→ ✓ excellent thermal conductivity (x15) → use as cooling structure
  ❖ large $w_i$ (x 3.6) → small signal charge
  ❖ fabrication not standard (wafer production, cutting) … but “pixellation” almost trivial

using pixel-specific ENC formulae (CSA+filter) and measurements with 100 GeV $\pi$

S/N per 0.1% $X_0$ → Si : diamond $\approx 1 : \sim 1.4$

✓ poly-CVD has been turned into 16 chip ATLAS modules

✓ sc-CVD sensors of few cm$^2$ size used as pixel detectors
sLHC Sensor R&D

**single crystal diamond pixel detector**

![Image of single crystal diamond pixel detector]

**beautiful Landau distributions**

![Graphs showing Landau distributions at different applied voltages](image)

- $V_B = 100\ V$
- $V_B = 400\ V$

**pCVD diamond (grain structure)**

- ![pCVD diamond grain structure](image)

**scCVD is like silicon**

- ![Correlation graph showing scCVD and Si](image)

- [M. Mathes et al.](reference)

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PSD8 Glasgow, 9/5/2008 – N. Wermes, Bonn
planar sensor R&D

- technology of choice for larger area (costs !)
- increase radiation tolerance ($10^{16} \text{ cm}^{-2}$ tough !)
- increase active area fraction
- large activity on Si materials
  - FZ/(M)CZ
  - p-type bulk (no type inversion)

- **trend:** $n^+$ on $n \rightarrow n^+$ on $p$ (FZ or MCZ)
  - pixel electrodes on junction side
  - single sided wafer processing (cost!)
  - no reverse annealing for CCE meas.
  - $\sim 30\%$ CC @ $10^{16} \text{ cm}^{-2}$ ($\sim 6000 \text{ e}^-$)

R&D proposals and projects for sLHC
Pixels at sLHC: radiation tolerance

note: $n_{eq}(Si)$ normalization (correct for diamond?) & diamond better in S/N terms

PSD8 Glasgow, 9/5/2008 – N. Wermes, Bonn
sLHC sensor R&D

a personal opinion

• 3D silicon and CVD diamond (especially scCVD) are attractive

✓ for small area pixel detectors (1st layer) where costs do not play a major role
✓ radiation hardness is the major issue
✓ S/N counts!
  ▶ high quality wafer production at vendors must still be shown
  ▶ scCVD diamond perhaps not an option on the sLHC time scale? (unfortunately)
  ▶ only small single chip pixel modules demonstrated for 3D and scCVD
✓ large pixel modules made with pCVD diamond

• for outer layers (fluence < $10^{15}$ cm$^{-2}$, area > 5 m$^2$) planar detectors are the choice

✓ promising Si material studies (trend $n^+$ in p FZ or MCz)
  ▶ building and radiation testing of real modules is due!
sLHC data rates

Hit inefficiency rises steeply with the hit rate

**Bottleneck:** congestion in double column readout

⇒ more local in-pixel storage (130 nm !)
>99% of hits are not triggered
⇒ don’t move them

![sLHC architecture FE-I4](image)

D. Arutinov, Bonn

Bottleneck

Column pair bus
Data transfer clocked at 20MHz

Sense amplifiers
End of column buffer 64 deep

**FE-I3 Column pair**

![Local Buffers](image)

Buffer & serialiser
Serial out

**FE-I4 Column pair**

Bonn
Genova
LBNL
NIKHEF

PSD8 Glasgow, 9/5/2008 – N. Wermes, Bonn
Hybrid Pixel: sLHC FE - Chip and Modules

- smaller pixel area (50 x 250 µm²)
  - smaller occupancy, better resolution
- larger chip (!)
  - lower cost in BB & FC (cost driver)
- larger active area fraction
  - better coverage in inner layers
- power reduction (~60% of FE-I3)

<table>
<thead>
<tr>
<th>Active Area</th>
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<tbody>
<tr>
<td>7.6mm</td>
<td>8mm</td>
<td>2.8mm</td>
</tr>
<tr>
<td>FE-I3</td>
<td>active</td>
<td></td>
</tr>
<tr>
<td>74%</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Active Area</th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>16.2mm</td>
<td>~200um</td>
<td></td>
</tr>
<tr>
<td>FE-I4</td>
<td>~2mm</td>
<td></td>
</tr>
<tr>
<td>~87%</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

IBM reticule

Single Chip Modules

Multi Chip Module

2x2 FE’S

inner layers
outer layers
(semi-) Monolithic Pixels

STAR@RHIC, superBelle, ILC
(Semi-) Monolithic Pixels Overview

• DEPFET Pixels
  • one transistor in pixel bulk
  • Q-collection in fully depleted bulk
  • R&D (for ILC) since > 10 years
  • recently (2008): a 2 layer detector for superBelle

• Monolithic Active Pixels (MAPS-epi)
  • Q collection in thin epi-layer
  • need tricks for full CMOS
  • R&D (for ILC) since ~ 10 years
  • 2 (or 3) layer detector for STAR@RHIC

• Monolithic Active Pixels (MAPS-SoI)
  • full CMOS in active area
  • Q - collection in fully depleted bulk
  • R&D started 2006

I will show a selection of current efforts
DEPFET pixels

- p-channel MOSFET in pixel on a fully depleted bulk
  - large signal
  - fast collection
  - small pixels (24 x 24 µm²)

- Internal gate (IG): deep (~1µm) n-implant is potential minimum for e⁻

- Signal electrons accumulate in IG and modulate the transistor current (g_q ~ 400 pA/e⁻)
  - low C_in, internal amplification → low noise

- Accumulated charge removed by CLEAR ("reset")
  - multiple R/O possible
    - external reset needed (no reset noise if CLEAR complete)

- Transistor off during signal collection
  - low power

- R/O of the (current) signal at transistor drains
  - steering & signal processing by external ICs

Collaboration: Aachen, Bonn, Heidelberg, MPI Munich, Karlsruhe, Prague, Valencia
DEPFET pixels: „rolling shutter“ frame R/O

- **1 row active**
  - (1) read signal + ped current
  - (2) CLEAR
  - (3) read pedestal current
  - Merge currents: (1) – (2)

- **All other rows OFF**
  - Still active for signals

  \[ \text{low power!} \]
  \[ (60 \text{ mW/cm}^2) \]
DEPFET pixels: some features

Developments are for ILC → superBelle

- **low noise**
  - 1.6 e\(^{-}\) for long shaping times (µs),
  - goal: ~200e for fast R/O
  - for ILC/superBelle R/O speeds (~12 MHz line rate)
  S/N = 120 for 450 µm thick sensors (test beam)
  → goal S/N = 20 - 40 for 50 µm thick sensors

- **irradiation** (0.9 Mrad \(\gamma\), 3 x 10\(^{12}\) p/cm\(^2\), 2 x 10\(^{11}\) n/cm\(^2\))
  - threshold shifts (~4 V) – can be compensated
    (note: only 1 transistor per pixel)
  - leakage current increase → 20 - 95 e\(^{-}\)

- **space resolution**: < 2 µm

- **material**: < 0.15% \(X_0\) per detector layer (50 µm thin)

prove thinning process (anisotropic deep etching)

see talk by Petr Kodys
DEPFET pixels for superBelle

Barcelona, Bonn, Göttingen, Heidelberg, Karlsruhe, MPI Munich, Prague, Santiago de Compostella, Valencia

to cope with hit rate (400 kHz/mm²) …

- larger pixels (50 x 75 µm²)
- read out at both sides and 4 pixels in parallel (x 8)
- 80 ns per row (sample/clear/sample)
- 1 Gbit/s module data rate
DEPFET pixels for superBelle: IP - resolution

Impact parameter resolution (µm) vs. momentum (GeV/c)

Simulation

Impact parameter resolution:
- 135 µm (present SVD2)
- 40 µm (DEPFET sBelle)

Momentum:
- 0.5 GeV/c
- 20°
- 40°
- 60°
- 80°
Sensor and signal processing are integrated in the same silicon wafer
- commercial CMOS technology standard

Signal created in low-doped epitaxial layer (~10-15 µm, e.g. AMS 0.35 µm)
- MIP signal <1000 electrons → challenge for IC design

Q - collection by thermal diffusion (~100 ns), reflective boundaries at p-well and substrate, collected at n-well/epi junction
→ charge spread to several pixels

100% fill-factor (note definition), thin (~50 µm)

Small pixel sizes (pitch 20 – 30 µm):
→ a “must” and a virtue → few µm resolution!

Only NMOS transistors possible in active area (due to n-well/epi collection diode)

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**MAPS vs Hybrid Pix**

<table>
<thead>
<tr>
<th>Feature</th>
<th>MAPS</th>
<th>Hybrid Pixel Sensors</th>
</tr>
</thead>
<tbody>
<tr>
<td>Granularity</td>
<td>+</td>
<td>-</td>
</tr>
<tr>
<td>Material budget</td>
<td>+</td>
<td>-</td>
</tr>
<tr>
<td>Readout speed</td>
<td>-</td>
<td>++</td>
</tr>
<tr>
<td>Radiation tolerance</td>
<td>-</td>
<td>++</td>
</tr>
</tbody>
</table>
MAPS-epi


many activities: France, UK, US, Italy
(MAPS, CAPS, FAPS …..)

**simplest (typical) case**

- readout successive frames and subtract (CDS)
- eliminate: base levels, 1/f noise, fixed pattern noise

do this either offline → slow
or on-chip → current R&D
MAPS-epi: CDS correlated double sampling readout

1st frame

2nd frame

 raw data after CDS

eliminate
• base levels
• 1/f noise
• fixed pattern noise

so far: done offline
R&D → on-chip!

still: correct for pedestal and common mode

from
D. Contarato

PSD8 Glasgow, 9/5/2008 – N. Wermes, Bonn
MAPS-epi: EUDET telescope

DESY, CEA, CERN, CNRS, MPI, Bonn, Heidelberg, Geneva, Bristol, INFN

S/N ~ 11

3.3 µm resolution
MAPS-epi ➔ meeting the challenge: **STAR@RHIC**

ladder with 10 MAPS sensors (~ 2.2 cm each)

**special feature goals**

- pitch 20 – 30 µm ➔ spatial resolution < 10 µm
- 50 µm sensors ➔ 0.28% radiation length/layer (!)
- small power budget ➔ 100 mW/cm²
- integration time goal: <200 µs (@ L= 8×10²⁷)
- must sustain 300 krad/yr and ~10¹³/cm² nₐₑq /yr

**groups**

- LBNL-Berkeley
- IPHC/DAPHNIA France
MAPS-epi @STAR: current status

several prototypes
- MimoSTAR 2&3 (AMS 0.35)
- Mimosa 8/16 (TSMC 0.25/AMS 0.35)

tested features
- 25 µm pitch, 128 x 32 pix
- analog versus digital R/O
digital faster (column parallel + MUX)
  but needs discriminators

- integration time still large (~ms)
  need 200 µs

- on-chip prototyped
  – in-pixel CDS
  – column level: discrimination
    zero suppression

- radiation: remove thick oxide near
  Q-collecting diode

Based on tests of several different prototypes
S/N>12 allows detection efficiency >99.6%

AMS 0.35

~750 e

Y. Degerli et al, IEEE TNS, vol 52, no 6, 2005, pp 3186 - 3193
MAPS-epi @STAR: current status

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- **on-chip** prototyped
  – in-pixel CDS
  – column level: discrimination
    zero suppression
- radiation: \(\rightarrow\) remove thick oxide near Q-collecting diode

\[ \varepsilon > 99\% \]

\[ \sim 10^{-5} \]

Mimosa 16 binary R/O

Achieved performance

Y. Degerli et al, IEEE TNS, vol 52, no 6, 2005, pp 3186 - 3193
Main improvement R&D

1. improve the charge collection (speed and completeness)

2. go to “full” CMOS also in active area
MAPS-epi with deep n-well (→ enlarge the n-well diode)

- Extended Deep N-well collecting electrode (STM 130 nm triple well CMOS)
  - obtain higher single pixel collected charge
  - protect charge loss to competitive N-wells
  - can use PMOS transistors too
- Complete single pixel processing chain (CSA + Shaper + Discr. + Logic) in active area
  - Fill factor (note definition) = DNW/total n-well area ~90% in the prototype structures

Pavia, Bergamo, Pisa: V. Re, G. Rizzo et al.

see talk by Gianluca TRAVERSI
• Ambitious goal: a monolithic pixel sensor with similar readout functionalities as with hybrid pixels (sparsification, time stamping)

• Proof of principle with APSEL chip prototypes (STM 130 nm triple well CMOS)

• APSEL4: 32x128 matrix, sparse R/O and time stamping
MAPS-epi with deep p-well (→ shield the PMOS N-wells)


- use deep p-implant (p-well) to shield the n-wells that contain PMOS transistors
- only diode n-well still exposed to charge from the epi-layer
- fill-factor is 100%
- deep-p cannot be made too small → pixel size not too small
- several designs with full signal processing submitted (>150 transistors) + tested o.k
  - e.g. CSA + shaper + comp. + logic
  - 50 µm pixel pitch
- first prototype tests encouraging
  - Q-collection in n-well diode increased by factor more than 2

INMAPS quadrupel well 0.18 µm CMOS process (6 metals)
MAPS-Sol

- **Sol**
  - A thin Si layer (~100 nm) isolated with SiO$_2$ (each transistor in its own isolated island, shallow trench isolation, no junctions to bulk)

- **MAPS-Sol**:
  - A bonded wafer with high-$\Omega$ substrate + low-$\Omega$ top Si, separated by a buried oxide layer
    - standard CMOS (NMOS, PMOS, MIM cap…) can be used
    - efficient use of area for electronics
  - vertical via contacts reaching through to implants in the high resistivity wafer
    - no bump bonding
    - small pixel size possible
  - use of handle wafer in partial or full depletion determined by backside voltage

MAPS-Sol

<table>
<thead>
<tr>
<th>MAPS</th>
<th>Sol vs epi</th>
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<tbody>
<tr>
<td></td>
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</tr>
<tr>
<td>Granularity</td>
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<td>Material budget</td>
<td>+</td>
</tr>
<tr>
<td>S/N</td>
<td>-</td>
</tr>
<tr>
<td>Level of maturity</td>
<td>+</td>
</tr>
</tbody>
</table>

full CMOS in active area charge collection in **fully depleted bulk**

see also talk by D. Contarato
MAPS-Sol


New initiative:
FERMILAB (R. Yarema, G. Deptuch et al.)
+ Japan + LBNL + Hawaii

with commercial vendors (not many !! ... “change in process flow”)
→ OKI (150 nm & 200 nm)

Status: prototype experience → feasibililty study
- many design variations submitted
  for HEP applications: single particle sensitivity
  for imaging applications: photon counting
  – full blown CMOS electronics
    CSA + shaper + discriminator + (counter)

e.g.: 64x64 pix, 26 μm
CSA + shaper + discr.
**the main problem:** back gate effect

fully depleted high-$\Omega$ part couples into the channel $\Rightarrow$ acts as second gate $\Rightarrow$ substrate biasing leads to transistor threshold shifts

**ideas:**
- need thicker buried oxide layer
- use less $V_{\text{back}}$ $\Rightarrow$ partial depletion
- use dense matrix of $p^+$ implants to lower potential at the surface
3D integration

- several (tiers) of thinned semiconductor layers interconnected to form a **monolithic unity**

- different layers can be made in **different technologies** (high ohmic sensor, BiCMOS, deep sub-μ-CMOS, SiGe, opto-process, …)

- **driven by industry**
  - reduced R,L and C → improves speed
  - reduced interconnect power, x-talk
  - reduced size

First initiative @ Fermilab

France (many groups)

Germany (MPI, Bonn) following
3D integration

**heavy R&D at Fermilab:** R. Yarema, G. Deptuch et al. readout chip with time stamping and sparsification

3 tiers (no sensor yet)

attempts with several foundries: Tezzaron, Chartered, IZM, RTI, Ziptronix, MITLL

VIP: layout view with 3D Design Tool by Micro Magic
3D integration

3D integration post – processing

... ICV = Inter Chip Vias
... TSV = Through Silicon Vias

- hole etching and chip thinning
- via formation with W-plugs
- 2.5 Ω/per via

MPI-Munich & IZM/Munich
- build demonstrator using ATLAS pixel chip and pixel sensors made using ICV + SLID technology

Bonn & IZM/Berlin
- use TSV for new sLHC-ATLAS module concepts
Conclusions

Hybrid pixels

- matured with LHC
- only choice for sLHC
- needs heavy R&D on:
  - sensor materials
  - ICs and modules
  - 3D integration

Monolithic

- first real detectors in focus
- “dream” is getting closer
- needs heavy R&D on:
  - full (CMOS) integration
  - radiation tolerance
Thanks for talk material and discussions

- Woitek Dulinski
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- Laci Andricek
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- Renato Turchetta
- Hans-Günther Moser
- Hans Krüger
- Fabian Hügging
- Marlon Barbero
- David Arutinov
- Giovanni Darbo
- Maurice Garcia-Sciveres
- Cinzia da Via’
- Valerio Re
- Harris Kagan
Backup Slides
Making thin Sensors

- A novel technology to produce detectors with thin active area has been developed and prototyped (L. Andricek)

1. implant backside on sensor wafer
2. bond wafers with SiO₂ in between
3. thin sensor side to desired thick.
4. process DEPFETs on top side
5. etch backside up to oxide/implant

first ‘dummy’ samples: 50μm silicon with 350μm frame

thinned diode structures: leakage current: <1nA/cm²
Input Characteristics before and after irradiation

- Drain current [μA]
- Gate voltage (V)
- Transconductance [μS]
- Drain current [μA]

$g_m$ for $W/L=3$ before and after irradiation

**$^{60}$Co irradiation**

<table>
<thead>
<tr>
<th>Irradiation</th>
<th>TID / NIEL fluence</th>
<th>$\Delta V_{th}$</th>
<th>$g_m$</th>
<th>$I_{Leak}$ in int. gate at RT(*)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gamma $^{60}$Co</td>
<td>913 krad / ~ 0</td>
<td>~-4V</td>
<td>unchanged</td>
<td>156 fA</td>
</tr>
<tr>
<td>Neutron</td>
<td>~ 0 / 2.4x10^{11} n/cm²</td>
<td>~ 0</td>
<td>unchanged</td>
<td>1.4 pA</td>
</tr>
<tr>
<td>Proton</td>
<td>283 krad / 3x10^{12} n/cm²</td>
<td>~-5V</td>
<td>~ -15%</td>
<td>26 pA</td>
</tr>
</tbody>
</table>

(*) 5..22 fA non irrad.
IZM SLID Process, ICV

Metallization SLID (Solid Liquid Interdiffusion)

- Alternative to bump bonding (less process steps “low cost” (IZM)).
- Small pitch possible (< 20 μm, depending on pick & place precision).
- Stacking possible (next bonding process does not affect previous bond).
- Wafer to wafer and chip to wafer possible.

ICV = Inter Chip Vias

- Hole etching and chip thinning
- Via formation with W-plugs.
- Face to face or die up connections.
- 2.5 Ohm/per via (including SLID).
- No significant impact on chip performance (MOS transistors).