

**Czech Technical University in Prague**



**Faculty of Electrical Engineering**

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# **Design of Readout Electronics for the Mini-matrix DEPFET Detector**

**DIPLOMA THESIS**

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**Návrh vyhodnocovacích  
elektronických obvodů pro  
malopixelové detektory  
DEPFET**

**DIPLOMOVÁ PRÁCE**

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I declare that I wrote my diploma thesis independently and exclusively with the use of the cited sources. I agree with lending and publishing the thesis.

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In Prague, May 20, 2008

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**Title: Design of Readout Electronics for the Mini-matrix DEPFET Detector**

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**Department:** Department of Microelectronics

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**Abstract:** This thesis discusses pixel detector DEPFET that has been developed for the International Linear Collider. The DEPFET is a sideward depleted detector based on a high-ohmic substrate. A MOSFET is integrated directly to each detector's pixel and it provides first charge amplification stage. This configuration has excellent noise parameters. The thesis then presents a flexible readout system for the DEPFET Mini-matrices that allows new measurements and detector structure optimization.

**Název práce: Návrh vyhodnocovacích elektronických obvodů pro malopixelové detektory DEPFET**

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**Abstrakt:** Práce pojednává o pixelovém detektoru DEPFET, který se vyvíjí pro International Linear Collider. DEPFET je detektor založený na stranově vyprázdněném vysoce ohmovém substrátu a MOSFET tranzistoru integrovaném přímo v každém pixelu. Ten vytváří první zesilovací stupeň a umožňuje tak dosáhnout především vynikajících šumových vlastností. Dále práce představuje návrh flexibilního měřicího systému pro malopixelové matice DEPFET, který umožní nová měření a optimalizace struktury detektoru.

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## Used Symbols

ILC	International Linear Collider
DEPFET	Depleted Field Effect Transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
CERN	European Organization for Nuclear Research
LHC	Large Hadron Collider
LEP	Large Electron Positron Collider
MOS	Metal Oxide Semiconductor
CURO	Current Readout Circuit
ASIC	Application-specific Integrated Circuit
CMOS	Complementary Metal–oxide–semiconductor
ADC	Analogue to Digital Converter
FPGA	Field-programmable Gate Array
PCB	Printed Circuit Board
USB	Universal Serial Bus
PCI	Peripheral Component Interconnect
TIA	Transimpedance Amplifier
SPI	Serial Peripheral Interface Bus
DAC	Digital to Analogue Converter
QSPI	Queued Serial Peripheral Interface
DSP	Digital Signal Processing
$\Delta E$	energy loss
$m_0$	particle mass
$E$	energy
$e$	elementary charge
$\epsilon_0$	dielectric coefficient
$c$	speed of light
$r$	radius of the circular path
$z$	depth in the detector substrate
$N_D$	doping concentration

$d$	total wafer thickness
$\epsilon_s$	dielectric constant of the semiconductor
$V$	voltage
$z_{min}$	depth of minimal potential
$V_{DS}$	drain to source voltage
$V_{GS}$	external gate voltage
$I_D$	drain current
$g_q$	internal amplification
$\delta I_D$	change of the current
$\delta Q$	collected charge
$\mu_h$	hole mobility
$L$	gate length
$V_{DS}^{sat}$	saturation voltage
$\Delta U$	voltage swing
$Q_{in}$	charge accumulated in the internal gate
$G$	gain of the source-follower stage
$C_{GD}$	gate-to-drain capacitance gain
$C_{GS}$	gate-to-source capacity because
$C_L$	load capacity
$q$	elementary charge
$g_m$	transconductance
$\tau$	setting time
$R_{in}$	input resistance
$I_{ped}$	pedestal current
$I_{sig}$	signal current
$SNR_{ADC}$	signal to noise ratio of the data acquisition card
$V_S$	input signal
$V_N$	input referred noise voltage
$ENOB$	effective number of bits of the ADC
$R_X$	resistance
$V_X$	voltage
$I_X$	current
$C_X$	capacitance

$L_X$	inductance
$A(s)$	voltage amplifier gain
$P_a$	transfer function pole
$s$	complex frequency
$Z(s)$	closed loop gain of the TIA
$BW$	bandwidth
$\Gamma$	reflection coefficient
$Z_0$	characteristic line impedance
$k$	Boltzman's constant
$T$	temperature in Kelvin
$i_N$	input noise current spectral density
$e_N$	input noise voltage spectral densities
$ENC$	Equivalent Noise Current
$E$	output-referred noise RMS voltage
$N(f)$	output-referred voltage spectral density
$D$	decimal equivalent of the binary code
$\nu$	temperature in °C
$t$	time

# Chapter 1

## Introduction

The International Linear Collider is a perspective project and many different countries and collaborations are participating on it to explore new secrets of particle physic. One of them is a DEPFET collaboration that is associating physicists and engineers, who are developing a new pixel semiconductor vertex detector for the ILC. The DEPFET (DEPLETED Field Effect Transistor) is the detector based on a fully depleted substrate and a MOSFET (Metal Oxide Semiconductor Field Effect Transistor) that is integrated directly in each pixel and providing first amplification stage. This configuration allows achieving excellent noise parameters and that is a reason why it's advantageous for low noise measurements.

Matrices with 64 x 128 pixels will be used for the ILC and prototypes have been produced and tested. For studying DEPFET parameters few types of Mini-matrices were designed up today. These prototypes are 3.5 x 3.5 mm large with 16 x 6 pixels and in contrast to the large matrices allow doing many precision measurements. Up today, studies on single pixel readout have been done [14] and now we are preparing a flexible Mini-matrix readout system. The Mini-matrix pixel readout system is based on the Single pixel readout system, but number of readout channels is increased to eight and the precision matrix switching is possible. The Mini-matrix readout is designed to make possible a precision collected charge measuring in each pixel with low noise, charge shearing among multiple pixels, clustering, charge-loss measuring, find optimal voltage values and timing of driving signals and should allow us to make a computer post-analysis as a correlated sampling and averaging.

This thesis is divided into 5 chapters. In Chapter 2 brief overview and preliminary design concept of the International Linear Collider is given. In Chapter 3 a description of the DEPFET detector and the readout electronics follows. The author's work is concentrated in Chapter 4. This chapter is about the readout

electronics and the switching circuits and presents the author's design and simulations of these circuits.

# Chapter 2

## International Linear Collider

In principle there exist two possible ways how to create large accelerators. One is to use a circular topology as used at CERN facilities as Large Hadron Collider (LHC) or older, the Fermilab proton anti-proton collider Tevatron and the Large Electron Positron collider (LEP) at CERN. In these colliders, particles are accelerated in a ring until they reach a designated energy and are then brought to collision. Since the ILC will use electron positron pairs to collide and energy up to TeV, the circular conception is not possible due to high energy losses by synchrotron radiation.

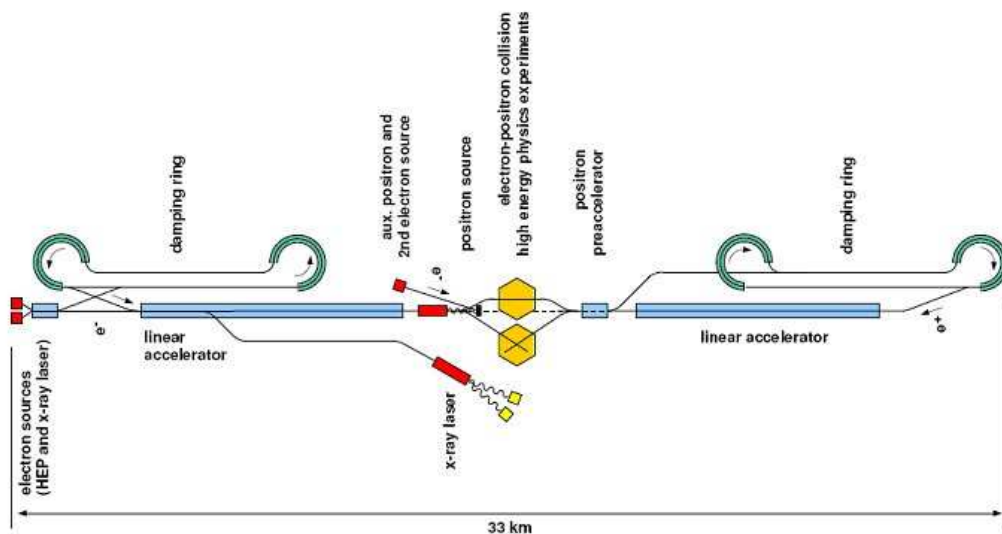


Figure 2.1 – Conception of the ILC [1]

The synchrotron radiation emitted by charged particle flying on the circular trajectory is proportional to  $1/m^4$ . The energy loss  $\Delta E$  due to synchrotron radiation for one circular revolution of a highly relativistic particle with rest mass  $m_0$  and energy  $E$  is given by [1]

$$\Delta E = \frac{e^2}{3\epsilon_0} \frac{E^4}{(m_0 c^2)^4 r}, \quad (2.1)$$

where  $e$  is the elementary charge,  $\epsilon_0$  is the dielectric coefficient,  $c$  is the speed of light and  $r$  is the radius of the circular path.

Another accelerator conception is the linear as shown in Figure 2.1 and is planned for the ILC. More detail description of the ILC is in [1]. In this case two particles start at the different places and they are accelerated in a straight line before they collide. There are no energy losses due to synchrotron radiation in this conception.

# Chapter 3

## DEPFET Sensor

### 3.1 DEPFET pixel structure

The DEPFET is an active pixel detector with internal signal amplification. It's based on a Field Effect Transistor (MOSFET), that is integrated directly to the each detector's pixel and it provides a first charge amplification stage. Detector itself consists of a high-resistivity depleted n-substrate and two p-regions, creating a pnp-sandwich structure (p frontside-implantation, n-substrate, p-backside). The n-substrate is sideward depleted.

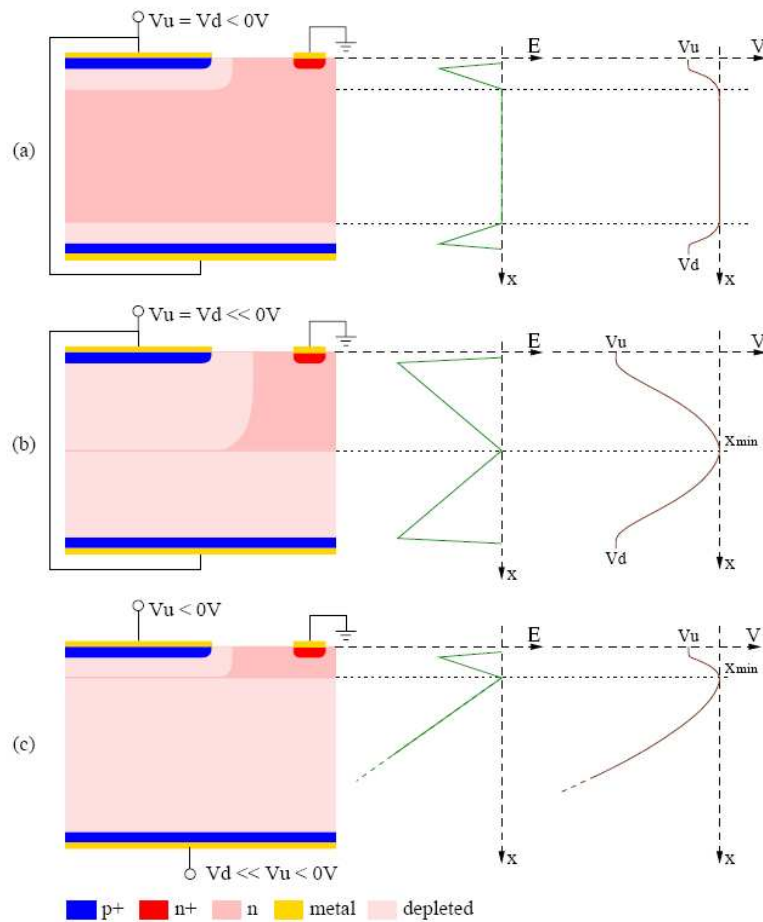


Figure 3.1 – Principle of the Sideward Depletion [3]

The principle of sideward depletion is shown in the figure 3.1 and is discussed in [1] and [3]. The n-substrate (bulk) is depleted from both sides by applying negative voltages to both p-implantations with respect to the bulk. The electron potential minimum is in a plane parallel to the front. We can write an one-dimension Poisson equation with boundary conditions  $\varphi(0) = V_u$  and  $\varphi(d) = V_d$

$$\varphi(z) = \frac{qN_D}{2\epsilon_s} z(d-z) + \frac{z}{d}(V_d - V_u) + V_u, \quad (3.1)$$

where  $z$  is the depth in the detector substrate,  $q$  is the elementary charge,  $N_D$  is the doping concentration of the substrate,  $d$  is the total wafer thickness,  $\epsilon_s$  is the dielectric constant of the semiconductor and  $V_d$ ,  $V_u$  are the voltages applied to the back and the front side. The minimum of the potential is in the depth  $z_{min}$  given by [1]

$$z_{min} = \frac{d}{2} + \frac{\epsilon_s}{qN_D d} (V_d - V_u). \quad (3.2)$$

If  $V_u = V_d$  the potential minimum will be in the middle. Applying asymmetric voltages is used in the DEPFET pixel to shift electron potential minimum close to the front surface, where is the MOSFET. Additional n-implants hinder electron lateral diffusion and electrons are concentrated in a small region under the MOSFET channel. This region is called an internal gate.

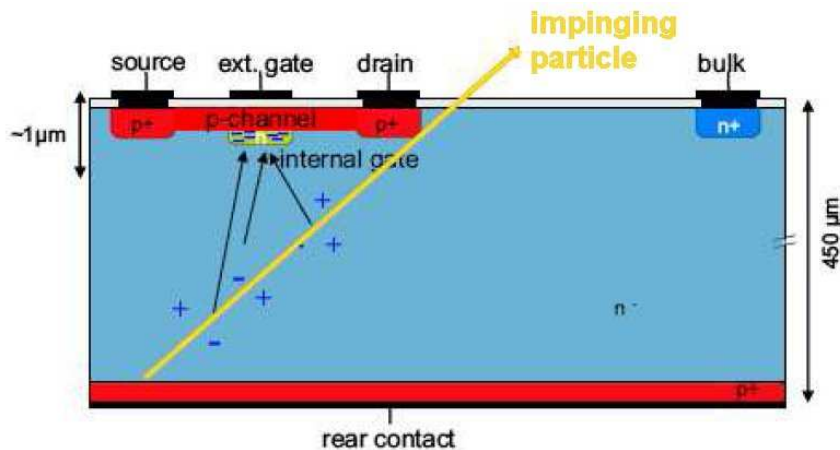


Figure 3.2 – The DEPFET Pixel Cross-section [1]

When an impinging radiation generates electron-hole pairs in the depleted n-substrate (bulk), the holes drift to the backside contact, but the electrons are trapped in the internal gate. Because the internal gate is located directly under the MOSFET channel under the external gate contact, so the stored charge in the internal gate affects MOSFET channel. It allows charge non-destructible reading and the reading process can be repeated many times. For a fixed drain to source voltage  $V_{DS}$  and a constant external gate voltage  $V_{GS}$  a drain current  $I_D$  is proportional to the stored charge in the internal gate. The amplification  $g_q$  is given by the change of the transistor current  $\delta I_D$  due to the collected charge  $\delta Q$  [1]

$$g_q = \left. \frac{\delta I_D}{\delta Q} \right|_{V_{GS}, V_{DS}} . \quad (3.3)$$

Internal amplification can be expressed [1]

$$g_q = -\frac{\mu_h}{L^2} V_{DS}^{sat} , \quad (3.4)$$

where  $\mu_h$  is the hole mobility,  $L$  is the gate length and  $V_{DS}^{sat}$  is the transistor saturation voltage. According to formula 3.4,  $g_q$  can be maximized choosing the small channel length  $L$ . The amplification 300 – 600 pA/e<sup>-</sup> is obtained for mini-matrices with channel effective length 4  $\mu\text{m}$ .

## 3.2 Clearing process

When a new charge collection is needed, it's necessary to empty the internal gate. For clearing out the internal gate, there is a clear contact next to the MOSFET transistor. In Figure 3.3 is a Cleargate cross-section and in Figure 3.4 is a top view the DEPFET structure. Detail description of the clearing process is in [6], [7], [8]

and [9]. The electrons are extracted from the internal gate by applying high positive voltage to the Clear contact. It causes the electrons drift to the Clear contact, where they are taken away. To prevent losses during charge accumulation, the  $n^+$ -region under the Clear contact is surrounded by p-well. The  $n^+$ -region is providing an ohmic contact to the Clear electrode and with the p-well a reverse biased PN junction that represents a potential barrier for the electrons in the internal gate. When the voltage applied to the Clear electrode is high enough, the depleted region in the p-well overcome through the p-well and touches the p-well boundary (punch-through effect [2]). In this moment there is no barrier for electrons in the internal gate and they are extracted.

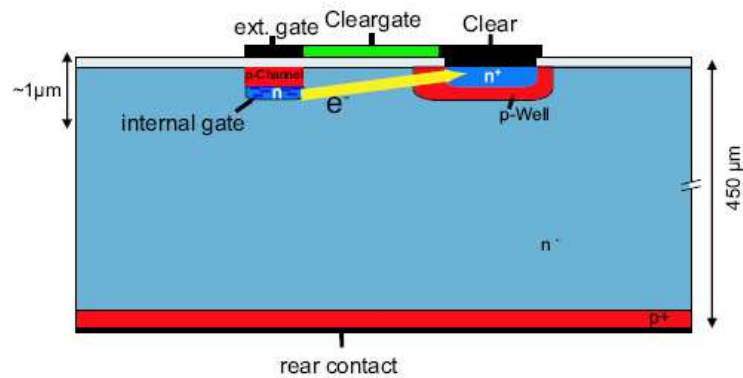


Figure 3.3 – Cleargate Cross-section [1]

In order to control the potential barrier between the internal gate and the Clear contact an additional MOS structure Cleargate is added. If the Cleargate is on a positive potential during the clear process, it helps forming an n-channel in the p-well. But whereas the n-channel is situated at the surface, the punch-through effect is also effective in the depths of the internal gate.

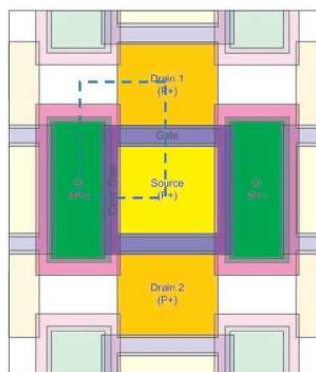


Figure 3.4 – The Double Pixel Layout [8]

It is possible to clock the Clear and the Cleargate as shown in Figure 3.5. This setting needs an extra control line for the Cleargate for each row. It's more efficient to find a static Cleargate operation potential. All Cleargates have a common contact, the Cleargate voltage is kept constant during whole operation and the clear process is controlled only by voltage at the Clear contact.

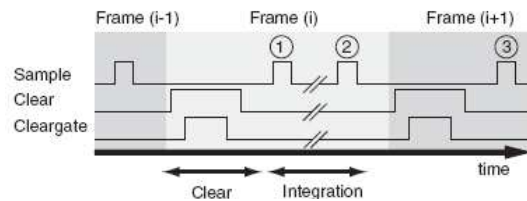


Figure 3.5 – Readout Scheme with the Cleargate Clocking [9]

As described in [9], the clearing process can be improved by an additional unmasked high energy  $n^+$ -implantation in the depth  $1.2 \mu\text{m}$  under the surface (it's not marked in Figure 3.3). It shifts the flow of electrons during the clear process deeper to the substrate and the punch-through is easier, because of lower capacitive coupling between the p-well and the Cleargate. It decreases the Cleargate-voltage swing and allows static Cleargate-voltage operation. A negative effect of the deep-energy  $n^+$ -implantation is a shift of the internal gate deeper underneath the surface and consequently reduction of the internal gain  $g_q$ .

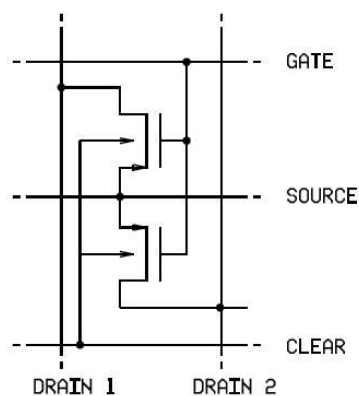


Figure 3.6 – The DEPFET Double Pixel [8]

### 3.3 DEPFET Matrix

As shown in Figure 3.4 and 3.6 the DEPFET matrix consists of double pixels. It means that two pixels have common source and a set of control lines (Gate and Clear). Thus the row clock rate can be half and the number of control lines is reduced. This parallelization increase number of readout channels, but it's advantageous because of compact layout.

Charge accumulation in each pixel is independent of external Gate-voltage and no pixel enabling is necessary. It allows a row-wise operation of the matrix. As shown in Figure 3.7, whole row (double-row) is selected by the Gate-voltage and readout in parallel or cleared by Clear-voltage. Two steering chips (Switchers) are attached on the both sides of the DEPFET matrix and drain currents are readout by a current readout circuit (CURO).

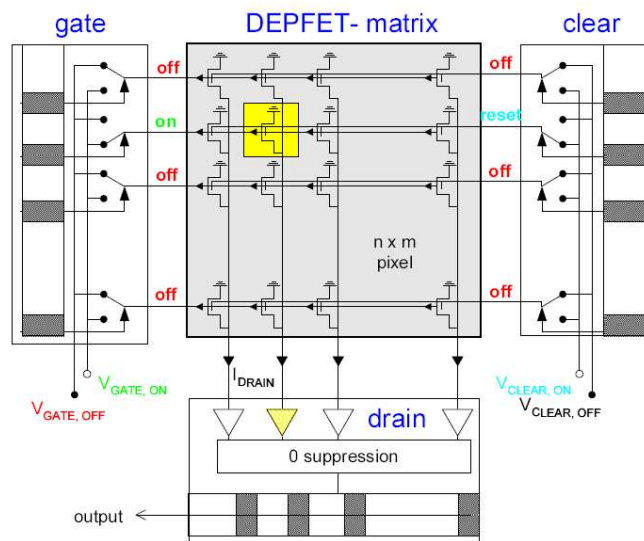


Figure 3.7 – The Row-wise Operation of the DEPFET Matrix [7]

## 3.4 DEPFET readout

### 3.4.1 Source-follower

The DEPFET detector makes possible two ways of readout as shown in Figure 3.8. The first is a voltage based readout using a source-follower configuration. The DEPFET transistor is biased by a constant current source and output signal is taken as a source voltage swing. The source voltage swing  $\Delta U$  is caused by charge accumulated in the internal gate  $Q_{in}$ . The gain  $G$  of the source-follower stage can be approximately expressed as [3]

$$G = \frac{\Delta U}{\Delta Q_{in}} = \frac{1}{C_{GD}}, \quad (3.5)$$

where  $C_{GD}$  is the gate-drain capacitance of the DEPFET detector. The gain is independent of the gate-to-source capacity  $C_{GS}$ , because  $V_{GS}$  is constant. The setting time  $\tau$  in which the output signal reaches 63% of its maximal value is approximately given by [3]

$$\tau \approx \frac{C_L \left( 1 + \frac{C_{GS}}{C_{GD}} \right) + C_{GS}}{g_m}, \quad (3.6)$$

where  $C_L$  is a load capacity of the output node and  $g_m$  is the transconductance of the DEPFET transistor. Because  $C_L$  is the capacity of the whole matrix column (approximately 10 pF), it dominates in the numerator of equation 3.6. The transconductance  $g_m$  of the transistor is limited by the gate length  $L$  technological limit 2  $\mu\text{m}$ . Consequently the setting time  $\tau$  is about of ones of  $\mu\text{s}$  and unacceptably long for the ILC operation.

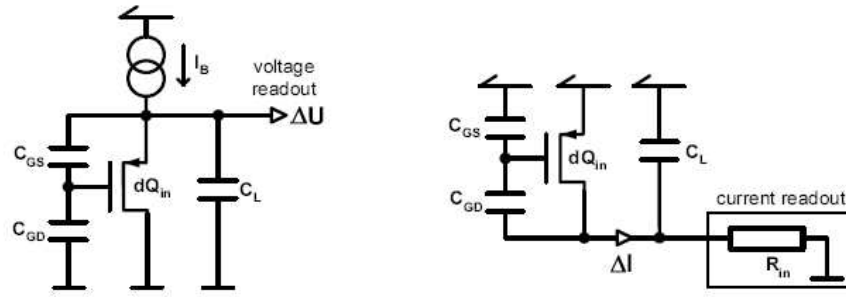


Figure 3.8 – The DEPFET Readout (Left: Source follower; Right: Drain current readout) [1]

### 3.4.2 Drain Readout

In case of the drain current readout the drain-source voltage is kept constant. As described in Chapter 3.1, the output current  $dI$  is given by accumulated charge  $dQ_{in}$  and amplification of the internal gate  $g_q$

$$dI_D = g_q dQ_{in}. \quad (3.7)$$

In this case the setting time  $\tau$  is independent of the DEPFET transistor transconduction  $g_m$  and is given by

$$\tau = C_L R_{in}, \quad (3.8)$$

where  $R_{in}$  is the input resistance of the readout electronics. In this configuration it is possible to decrease setting time up to  $\tau = 1$  ns and it's acceptable for the ILC operation. Since the fast operation is crucial for the ILC operation the current read operation was chosen.

### 3.4.4 ASIC Readout Chips

Up today two prototypes of ASIC current readout chips were designed. In Figure 3.9 are photographs of readout chips CURO I and CURO II. The circuit is based on current memory cells and analog current subtraction.

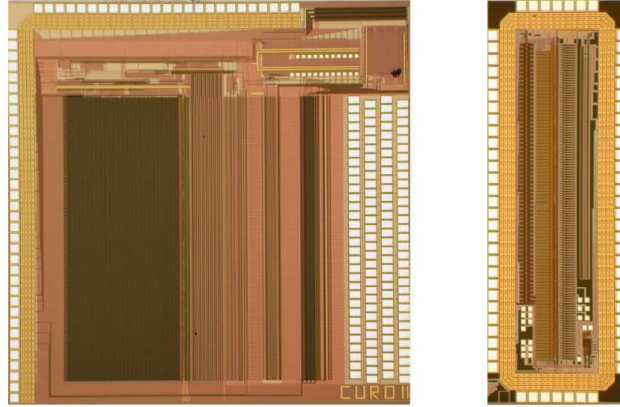


Figure 3.9 - Micro Photograph of the  $4.5 \times 4.5\text{mm}^2$  CURO II chip (left) and the  $1.5 \times 4\text{mm}^2$  Prototype Chip CURO I (right) Fabricated in a  $0.25 \mu\text{m}$  Process [1]

In Figure 3.10 is a scheme of readout at the ILC discussed in [1]. The matrix is readout row-wise at 20 MHz frequency. In the first step the row is cleared and a pedestal current  $I_{ped,i}$  is sampled. After an integration time, when others rows are processed, the row is selected again and the signal current with the pedestal current  $I_{sig,i} + I_{ped,i}$  is sampled. By subtracting both values  $I_{sig,i} = (I_{sig,i} + I_{ped,i}) - I_{ped,i}$  the signal current is obtained. If the pedestal current is constant during few frames  $I_{ped,i} = I_{ped,i+1}$  then readout can work according to the scheme (Figure 3.10) and the signal current is given by

$$I_{sig,i} = (I_{sig,i} + I_{ped,i}) - I_{ped,i+1}. \quad (3.9)$$

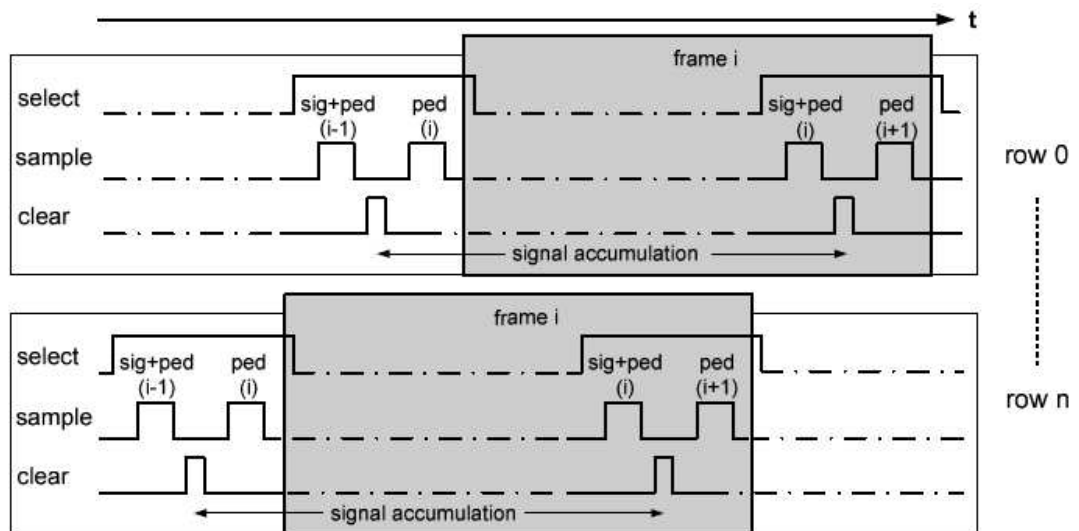


Figure 3.10 – Readout Scheme at the ILC [1]

### 3.5 DEPFET Switching Circuits

The DEPFET matrix is readout row-wise, so each row has to be addressed during the reading process. This is providing SWITCHER chip [18] that is switching each matrix rows. The second SWITCHER chip is providing the Clear control signals. Up today, three versions of ASIC SWITCHER circuit were produced. The circuits are made in CMOS technology and they are able to switch voltages up to 10 V due to three stacked high voltage switches (Figure 3.11).

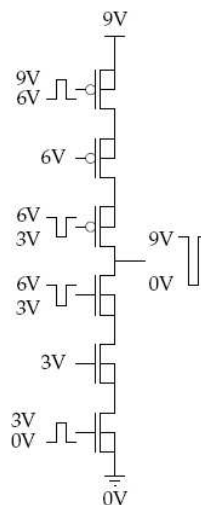


Figure 3.11 – The CMOS High Voltage Switch [18]

# Chapter 4

## DEPFET Mini-matrix Readout System

### 4.1 Mini-matrix Readout and Switching Circuit

#### Requirements

The Mini-matrix is a small (3.5 x 3.5 mm) prototype of the DEPFET sensor with 16 x 6 pixels. It was designed to study behaving of the DEPFET structures and processes during sensor operation. The internal pixel amplification  $g_q$  of the Mini-matrix is between  $300 \div 600 \text{ pA/e}^-$  and the output capacity of the whole line is approximately 10 pF.

The Mini-matrix readout setup should allow us to make a precision collected charge measuring in each pixel with low noise, charge shearing among multiple pixels, clustering, charge-loss measuring, find optimal voltage values and timing of driving signals and should allow us to make a computer post-analysis as correlated sampling, averaging, etc. From the previous points flow requirements for the readout electronics:

- Total input noise below  $20 \text{ e}^-$  (electrons)
- 14-bit ADC with 100 Msps for each channel
- Frame readout time  $20 \mu\text{s}$
- Gate and Clear voltage setting time below 50 ns
- Possibility of Gate voltages timing with resolution of 5 ns and allow Gate signals overlapping
- Digitally reconfigurable subtracting voltage for the pedestal current subtraction

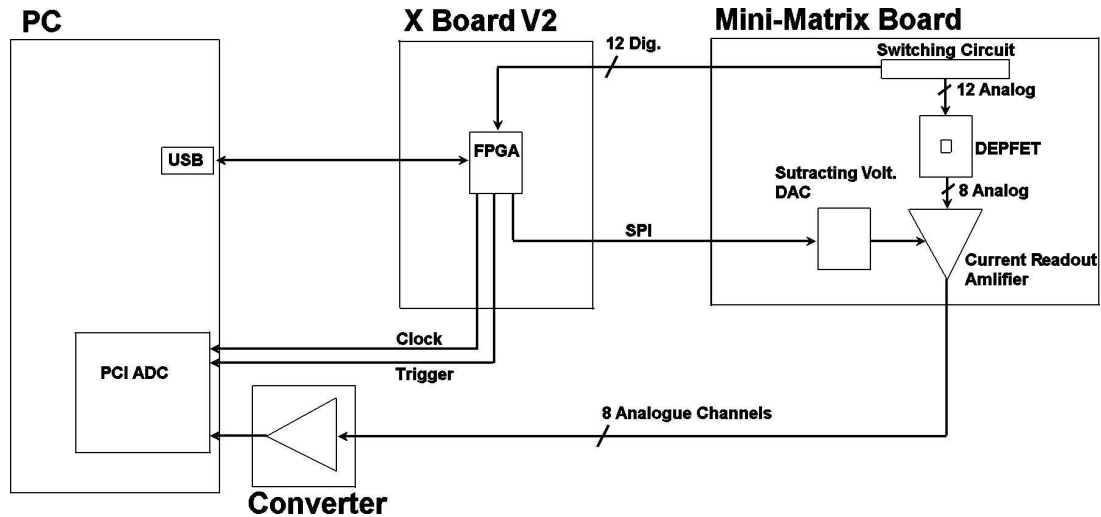


Figure 4.1 – Conception of the Mini-matrix Readout System

## 4.2 Measuring System Conception

Figure 4.1 shows a block diagram of the measuring system. The system is made of four main blocks. A PC with an 8-channel 14-bit 100 Msps PCI data acquisition card, X Board V2 FPGA control card (Figure 4.2), a current readout and a switching circuit and a differential to single-ended converter. The data acquisition ADC card is a commercial PC card OCT-838-007 that is suitable for our solution. The ADC card is processing 8 parallel analog signals from the current readout amplifiers. It needs to be synchronized with the rest of the system circuits, so the ADCs are clocked and triggered externally by the FPGA control card. The current readout circuit is providing the drain current readout of the DEPFET sensor and it's placed together with the switching circuit on the same PCB. The current readout circuit is made of 8 drain readout amplifiers and the switching circuit contains 12 individual analog switches that are necessary to control the Gate and Clear electrodes of the DEPFET Mini-matrix sensor. The X Board v2 is the FPGA card with a Xilinx's Vertex 2 FPGA chip that was made in the Max-Planck Institute in Munich. The FPGA chip on the X Board provides communication with the PC via a USB port. The board is also providing the clock and the trigger signals for the ADCs, digital signals for the

current readout amplifiers setting. The FPGA also contain a sequencer circuit that generates flexible and precision driving signals for the switching circuit.

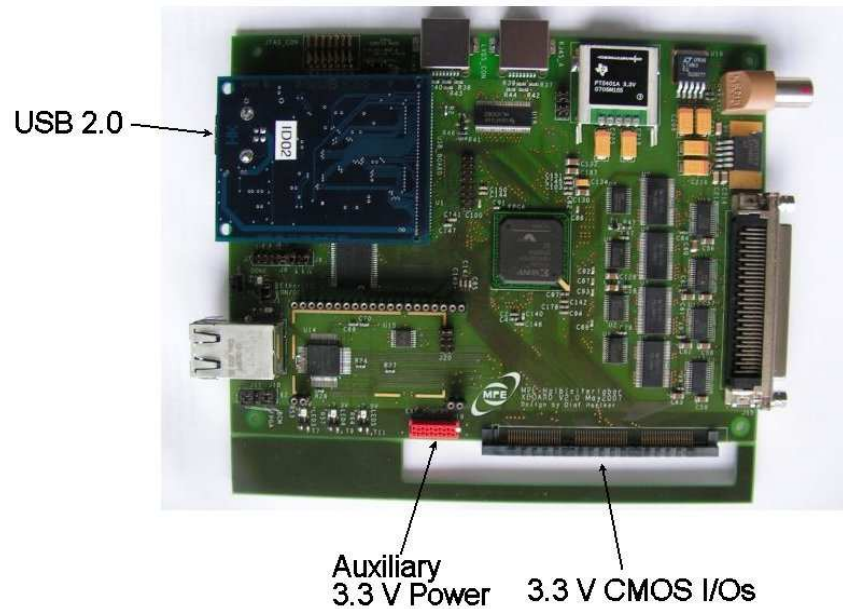


Figure 4.2 – X Board v2

The DEPFET detector itself is contacted to the 40-pin ceramic holder. A photograph of the ceramic holder is shown in Figure 4.3. The holder is plugged into a ZIP socket on the PCB. The capacity of each wire is approximately 10 pF and serial inductance 100 nH.

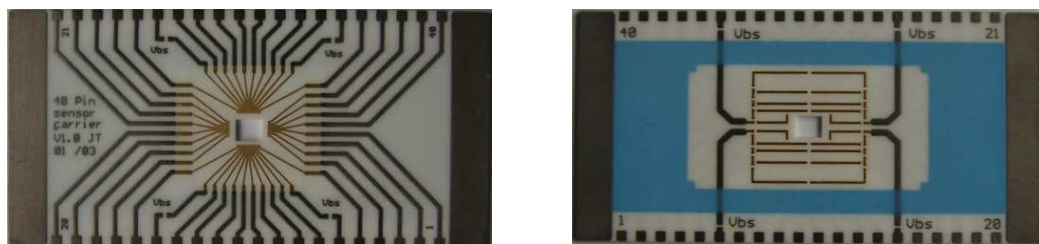


Figure 4.3 – The 40-pin Ceramic Holder (Left: Top view; Right: Bottom view)

## 4.3 Data Acquisition Card

For data acquisition was chosen GaGe PCI Octopus Card OCT-838-007 described in [19]. It is a multi-channel digitizer single-slot PCI card. This card is providing following features

- 8 digitizing channels
- 100 MS/s sampling per channel
- 14 bits vertical resolution
- 128 MS to 2 GS on-board acquisition memory
- More than 100 MHz bandwidth
- Full-size, single-slot PCI card
- Front-end system, with software control over input ranges, coupling and impedances
- 32 bits, 66 MHz PCI standard for 200 MB/s transfer to PC memory
- External or reference clock in and clock out, external trigger in and trigger event out
- Programming-free operation with oscilloscope software
- Software development kits available for LabVIEW, MATLAB, C/C#



Figure 4.4 – The Data Acquisition Card [19]

Figure 4.5 shows a block diagram of the data acquisition card. It consists of front-end amplifiers with reconfigurable gain, selectable input impedance  $1\text{ M}\Omega$  or  $50\ \Omega$  and DC or AC coupling. Then follow high speed ADCs. Output from the

ADCs is digitally processed in the FPGA chip and results can be temporarily stored in an internal memory or sent via PCI controller to the PC. The system has advanced triggering options and clock synchronization and PC software support.

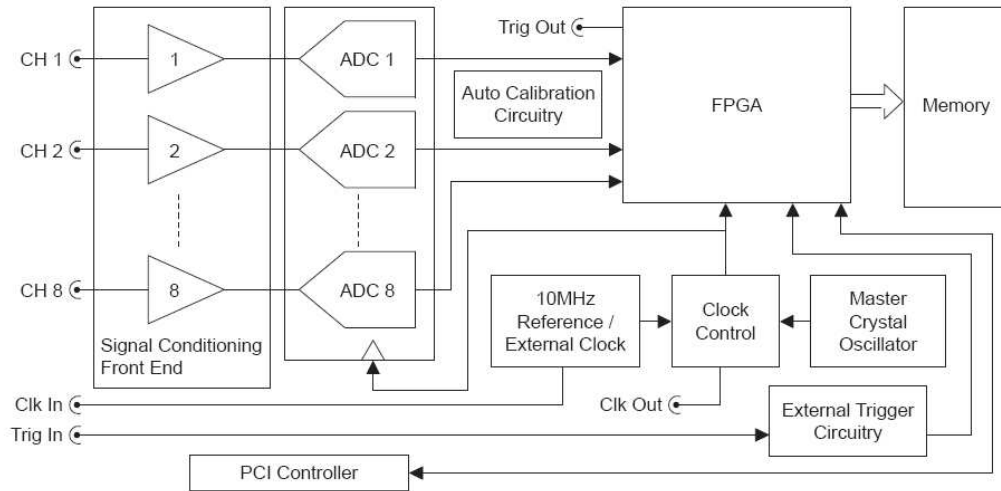


Figure 4.5 – The Data Acquisition Card Block Diagram [19]

The signal to noise ratio  $SNR_{ADC}$  of the data acquisition card is 68 dB. Definition of the  $SNR_{ADC}$  is [17]

$$SNR_{ADC} = 20 \log \left( \frac{V_S}{V_N} \right), \quad (4.1)$$

where  $V_S$  is an input signal of 95% of a full scale amplitude and  $V_N$  is an input referred noise voltage. An effective number of bits of the ADC  $ENOB$  is given by an empiric equation [17]

$$ENOB = \frac{SNR_{ADC} - 1.76}{6.02}. \quad (4.2)$$

If  $SNR_{ADC} = 68$  dB then  $ENOB = 11$  bits. The effective number of bits will be increased by additional software operations as averaging.

## 4.4 Current Readout Amplifier

In Figure 4.8 is a DEPFET readout amplifier. It consists of 3 parts, TIA, non-inverting operational amplifier (EL2126 [11]) and fully differential output buffer (AD8139 [12]). The DEPFET signal consists of two parts, a signal current and a pedestal current. A charge accumulated in the internal gate has no affect to the pedestal current, so it's advantageous to subtract the pedestal current at the analog level. It's simply done through the  $R_7$ . The drain voltage at the non-inverting input of the operational amplifier is kept at  $-5\text{V}$  (a virtual drain voltage  $V_2 = -5\text{ V}$ ) and the voltage drop at the subtracting resistor  $R_7$ , caused by the pedestal current flow, is compensated by a subtracting voltage source  $V_1$ . This voltage source is digitally adjustable with 10-bit resolution as described in Chapter 4.6. The input current flows only thru the feedback resistor  $R_1$ . It means that the amplification of the first stage (transimpedance amplifier) is given only by resistance of the feedback resistor  $R_1$ . The TIA output voltage  $V_{OUT}$  can be expressed according to the following formula

$$V_{OUT} = -I_{IN}R_1, \quad (4.3)$$

where  $I_{IN}$  is the input current. Problem is that the input capacity  $C_3$  tends to make circuit unstable. As the signal runs along the feedback path from output to input,  $R_1$  and  $C_3$  create a low-pass filter. And filters of the low-pass kind contribute negative phase to the feedback loop, making the circuit less stable or make even oscillations. Restoring stability requires counteracting the undesirable low-pass filter  $R_1$  and  $C_3$  in the feedback path from output to input. It can be done with a high-pass filter in the same feedback path by adding a capacitor  $C_1$ . The High-pass filter,  $C_1$  and  $R_1$ , adds positive phase to the loop pushing the circuit toward stability.

The TIA is a shunt-shunt voltage amplifier with a resistive feedback. Assuming that the voltage amplifier gain  $A(s)$  is expressed by the equation [4],

$$A(s) \cong \frac{-A}{1 + \frac{s}{P_a}}, \quad (4.4)$$

where  $A$  is an amplifier voltage gain,  $P_a$  is a transfer function pole and  $s$  is a complex frequency. The overall closed loop gain for this TIA  $Z(s)$  can be approximated by the equation [4]

$$Z(s) \cong \frac{R_1}{\left(1 + \frac{s(C_3 + C_{in})R_1}{A}\right) \left(1 + \frac{s}{P_a}\right)}, \quad (4.5)$$

where  $R_1$  is the feedback resistor  $C_3$  is the DEPFET output capacity and  $C_{in}$  is the input capacity of the operational amplifier. The transimpedance  $Z(s)$  has two poles. The first pole is related to the input node with total capacitance of  $C_{in} + C_3$ . The second pole  $P_a$  is due to amplifier itself, which is usually located at the output node. The dominant pole is the first one at the input node, and to ensure stability the second pole  $P_a$ , needs to be at much higher frequencies, at least 3 times higher. The 3-dB bandwidth  $BW$  of the TIA is approximately then [4]

$$BW \cong \frac{A}{R_1(C_3 + C_{in})}. \quad (4.6)$$

The second non-inverting stage allows trimming the offset voltage and increases the amplification of the whole readout amplifier. The amplification of the TIA cannot be too high due to the bandwidth limitation. The amplification of the second stage  $A_2$  is given by

$$A_2 = 1 + \frac{R_{12}}{R_{10}}, \quad (4.7)$$

where  $R_{10}$  and  $R_{12}$  are the feedback resistors.

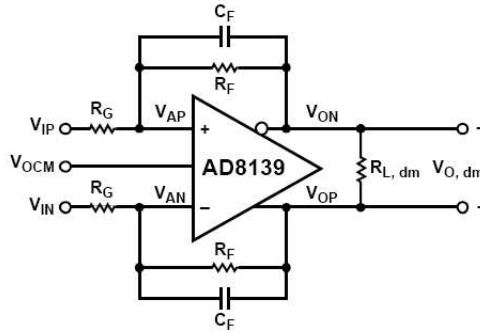


Figure 4.6 – Fully differential driver [12]

The third stage is the fully differential low noise ADC driver described in [12]. It's working in non-inverting configuration with the unit gain. More details are in [5]. Values of the resistors  $R_6$  and  $R_{11}$  are equal just as values of the resistors  $R_2$  and  $R_9$  (see Figure 4.8) and we mark  $R_6 = R_{11} = R_G$  and  $R_2 = R_9 = R_F$ . Figure 4.6 shows the notation of voltages. The differential output voltage  $V_{O, dm}$  is defined as

$$V_{O, dm} = V_{OP} - V_{ON}, \quad (4.8)$$

where  $V_{OP}$  and  $V_{ON}$  are the positive and negative output voltages. The differential negative feedback drives the voltages at the summing junctions  $V_{AN}$  and  $V_{AP}$  to be essentially equal to each other

$$V_{AN} = V_{AP}. \quad (4.9)$$

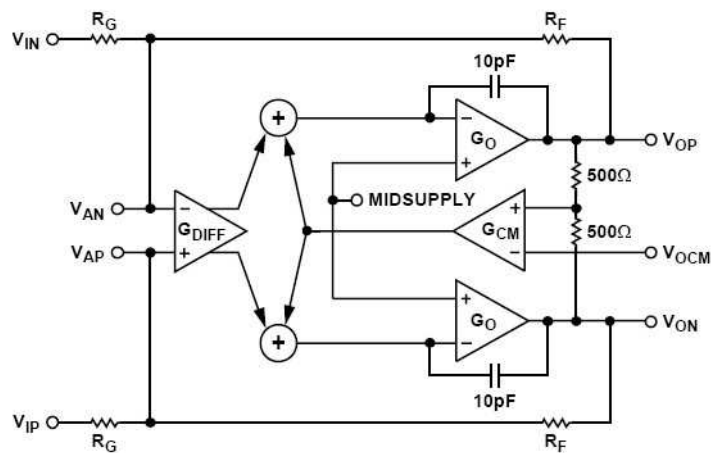


Figure 4.7 – Block Diagram of the Fully Differential Driver [12]

Function of the common output voltage pin  $V_{OCM}$  is shown in the block diagram of the fully differential driver (see Figure 4.7). The common-mode feedback loop drives the output common-mode voltage, sampled at the midpoint of the two  $500\ \Omega$  resistors, to equal the voltage set at the  $V_{OCM}$  terminal. This ensures that

$$V_{OP} = V_{OCM} + \frac{V_{O,dm}}{2}, \quad (4.10)$$

and

$$V_{ON} = V_{OCM} - \frac{V_{O,dm}}{2}. \quad (4.11)$$

The voltage gain of the single-ended to differential output topology can be deduced from the previous definitions. Referring to Figure 4.6 and setting  $V_{IN} = 0$  we can write

$$\frac{V_{IP} - V_{AP}}{R_G} = \frac{V_{AP} - V_{ON}}{R_F}, \quad (4.12)$$

$$V_{AN} = V_{AP} = V_{OP} \left( \frac{R_G}{R_F + R_G} \right). \quad (4.13)$$

Solving equations 4.12 and 4.13 gives the gain of the third stage  $A_3$

$$A_3 = \frac{V_{O,dm}}{V_{IP}} = \frac{R_F}{R_G}. \quad (4.14)$$

Another very important thing is a termination at source and load side of a transmission line between the output buffer and the ADC input. This problem is described in [15]. If the characteristic line impedance is  $Z_0$  and the line is terminated by a load resistor  $R_L$  so a part of an incident wave is reflected back with a reflection coefficient  $\Gamma$  that is given by [15]

$$\Gamma = \frac{V_r}{V_i} = \frac{R_L - Z_0}{R_L + Z_0}, \quad (4.15)$$

where  $V_r$  is the reflected wave amplitude and  $V_i$  is the incident wave amplitude. The same effect occurs also at the front side of the transmission line that is terminated by the output resistance of the output driver  $R_S$ . The reflections at the source and load side of the transmission line could distort signal especially at high frequencies or with short pulse rising and falling times. Such distortion is unacceptable for the precision measurements. If the  $R_S = R_L = Z_0$  the transmission line is matched and no reflections occur. The real transmission line has characteristic impedance  $50 \Omega$  and is terminated by a  $50 \Omega$  resistor that is parallel to a high impedance amplifier input. The output resistance of the line driver itself is very low so two additional serial  $25 \Omega$  resistors  $R_3$  and  $R_8$  (see Figure 4.8) are added to the output to match the  $50 \Omega$  line. The impedance matching network creates a voltage divider with a dividing factor  $A_4 = 1/2$ . The total transimpedance  $R_{TOT}$  of the whole chain is then given by

$$R_{TOT} = R_1 A_2 A_3 A_4. \quad (4.16)$$

Solving equations 4.7, 4.14 and 4.16 the  $R_{TOT}$  can be expressed by

$$R_{TOT} = \frac{R_1 R_F R_G (R_{10} + R_{12})}{2 R_{10} R_G^2}. \quad (4.17)$$

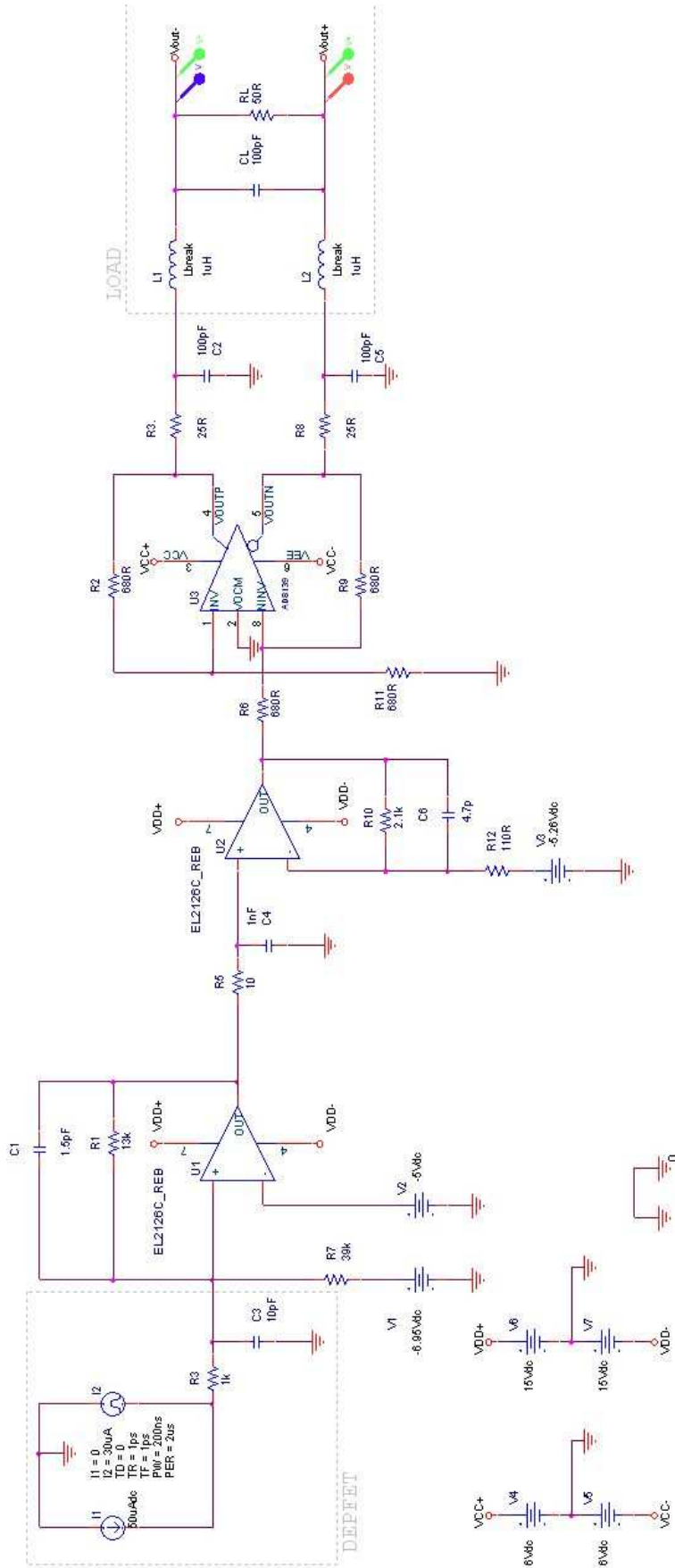


Figure 4.8 – Schematic of the Readout Amplifier, DEPFET and a 50  $\Omega$  Load

## 4.5 Computer Analysis

In Figure 4.9 is an electrical model of the DEPFET sensor used for simulations made in the PSpice. [15] discusses PSpice models and simulations. The DEPFET model consists of two current sources  $I_1$  and  $I_2$ . The  $I_2$  is the 50  $\mu\text{A}$  DC pedestal current and  $I_1$  is the pulse source that represents a signal current. The  $C_3$  represents output capacitance and the  $R_3$  channel and metallization resistance.

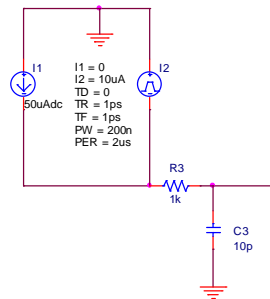


Figure 4.9 – Model of the DEPFET Pixel

The simulated circuit of the readout amplifier is shown in Figure 4.8. Expected maximal signal current is up to 30  $\mu\text{A}$  and the readout amplifier is designed to maximal differential output voltage 4 V. Virtual drain voltage  $V_2 = -5$  V. The TIA offset is compensated by the offset voltage  $V_3$ . Figure 4.10 shows relation between the output voltage and the offset voltage  $V_3$  when the input signal current  $I_2 = 0$  A. The zero output voltage offset is achieved when  $V_3 = -5.26$  V. In Figure 4.11 is shown a result of transient analysis with short input current pulses. Figure 4.12 shows a result of  $I_1$  DC sweep up to 40  $\mu\text{A}$ . The simulated transconductance of the readout amplifier is 130  $\text{k}\Omega$  that satisfies 30  $\mu\text{A}$  maximal input current and 4 V differential output. The frequency characteristic is shown in Figure 4.13. Due to noise reduction is the bandwidth limited by a simple low-pass filter  $R_5$   $C_4$  to 6 MHz.

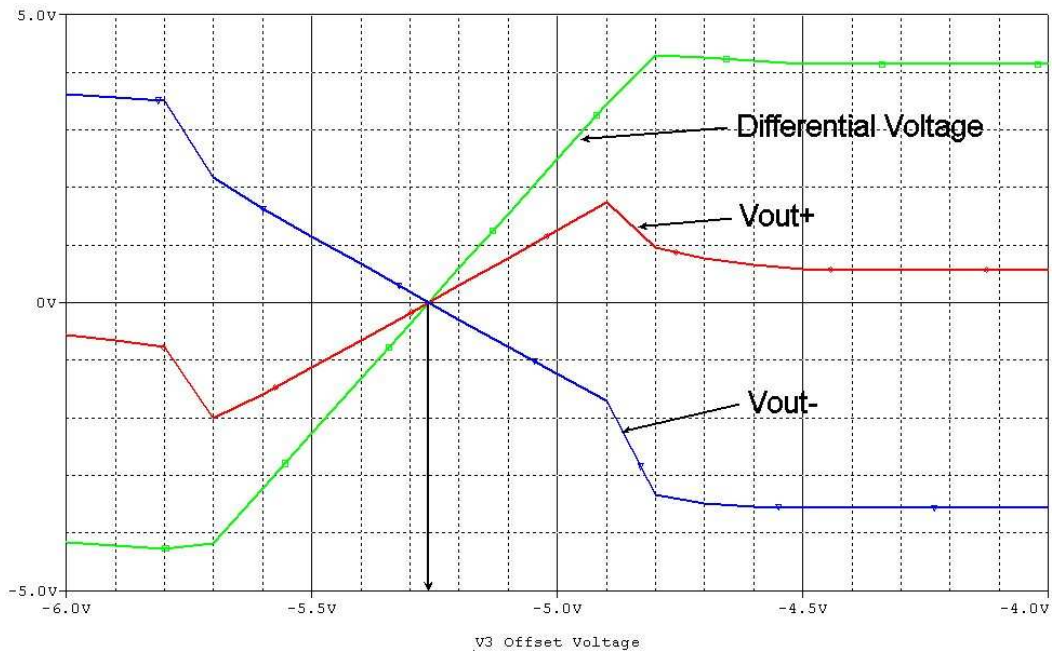


Figure 4.10 – The Offset Voltage Sweep

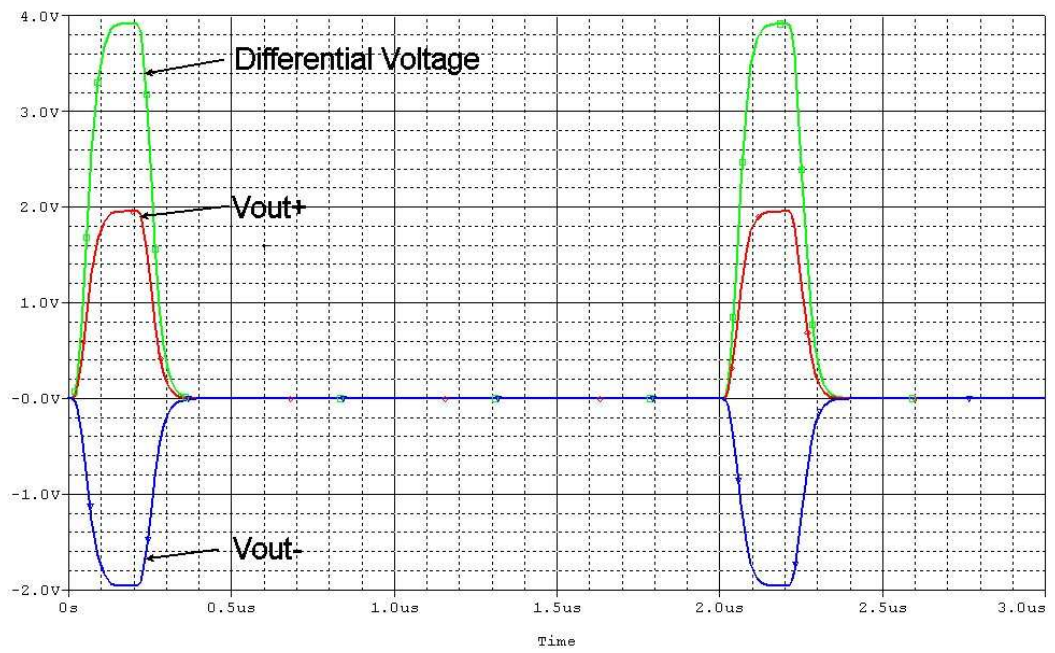


Figure 4.11 – Transient Analysis

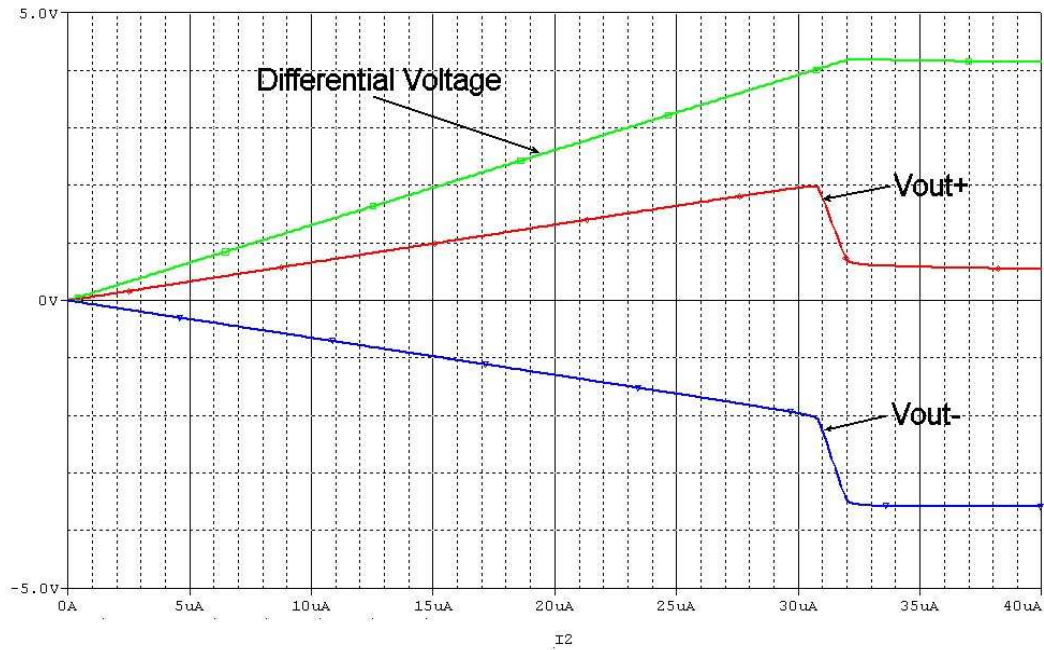


Figure 4.12 – DC Sweep

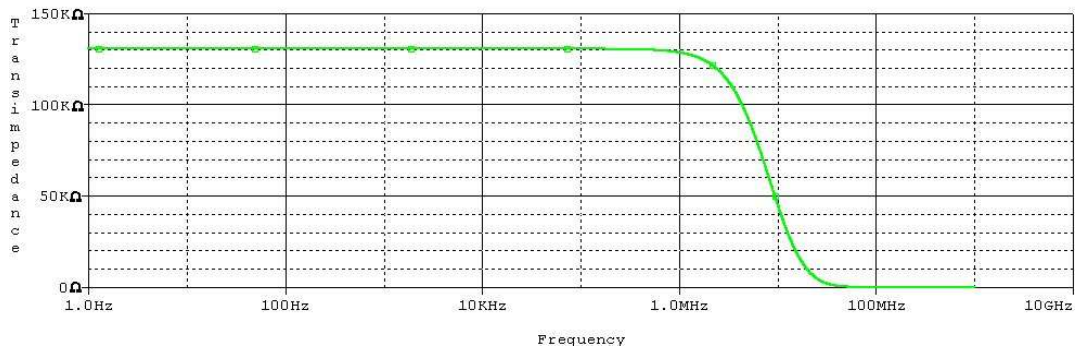


Figure 4.13 – AC Sweep

To estimate an amplifier's noise there are several points that complicate the simple analysis.

- The various noise sources operate over different bandwidths and determining these bandwidths requires rigorous calculation.
- Individual transfer function calculations from each source to the output are not trivial and are also frequency dependant.
- Amplifier parasitic elements, such as input common mode capacitance, affect frequency response and therefore noise bandwidth.

These requirements can be solved by a computer simulation in PSpice. The PSpice model with indispensable noise sources shown in Figure 4.14 simulates the output-referred noise voltage. Noise simulation is discussed in [16]. The  $i_{R1}$  and  $i_{R8}$  are corresponding resistor input-referred noise thermal currents densities. The thermal noise current density is given by [16]

$$i_R = \sqrt{\frac{4kT}{R}}, \quad (4.18)$$

where  $k$  is the Boltzman's constant,  $T$  is the temperature in Kelvin and  $R$  is the resistance. The  $i_N$  is the input noise current spectral density of the operational amplifier and  $e_{N1}$  and  $e_{N2}$  are the input noise voltage spectral densities of the operational amplifiers. In Figures 4.15 – 4.19 are output-referred noise voltage spectral densities for each noise source.

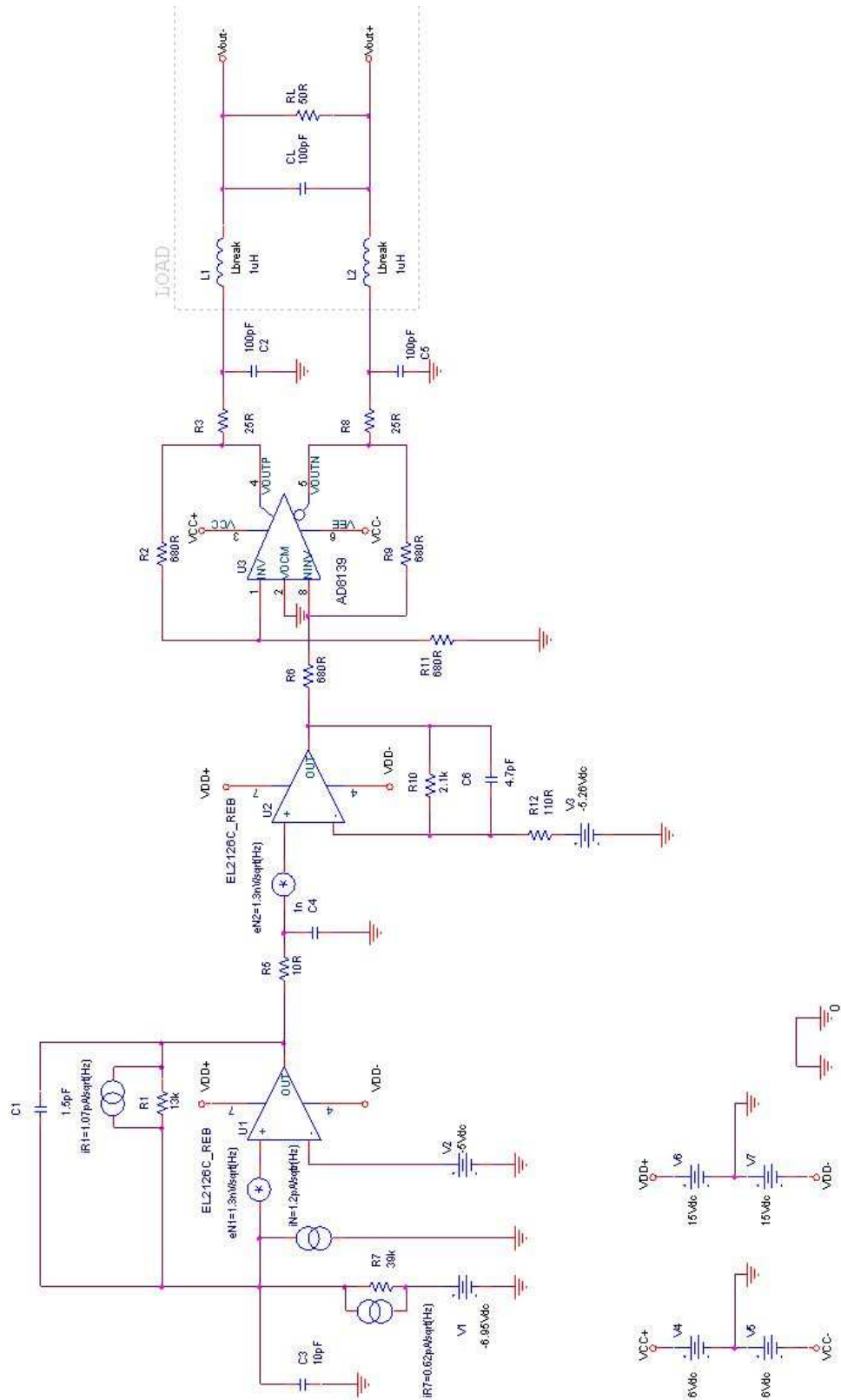


Figure 4.14 – Noise Model

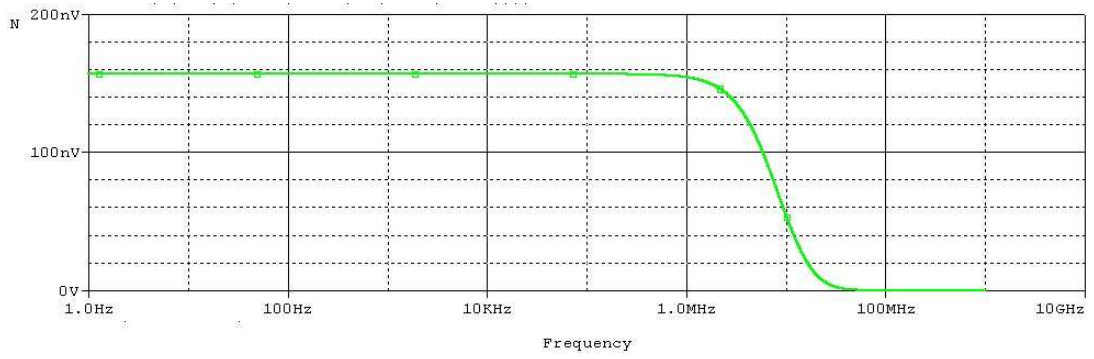


Figure 4.15 – Output-referred voltage spectral density of  $i_N$  noise source

$$N(f) \text{ [V}/\sqrt{\text{Hz}}]$$

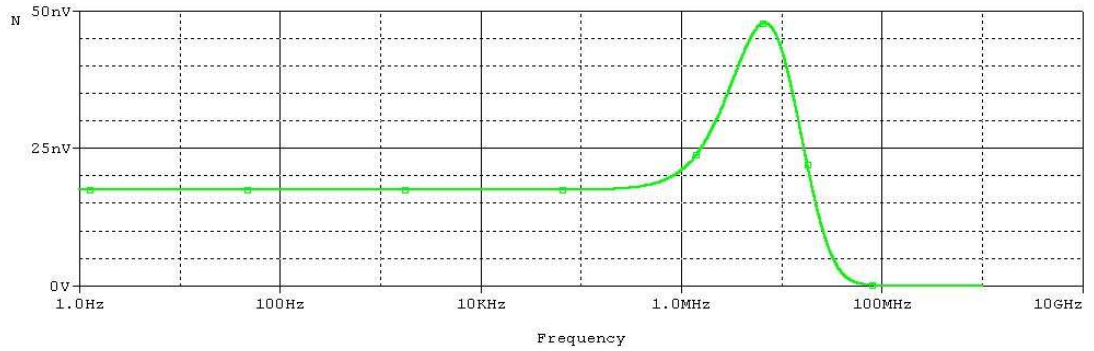


Figure 4.16 – Output-referred voltage spectral density of  $e_{NI}$  noise source  $N(f)$

$$\text{[V}/\sqrt{\text{Hz}}]$$

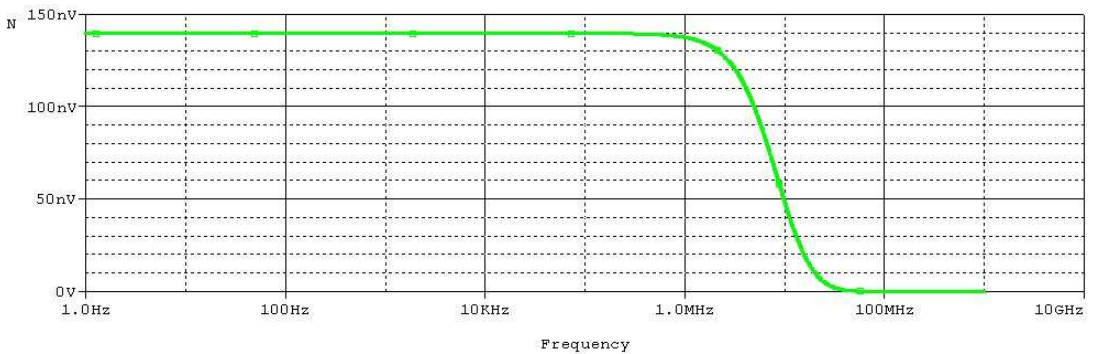


Figure 4.17 – Output-referred voltage spectral density of  $i_{RI}$  noise source  $N(f)$

$$\text{[V}/\sqrt{\text{Hz}}]$$

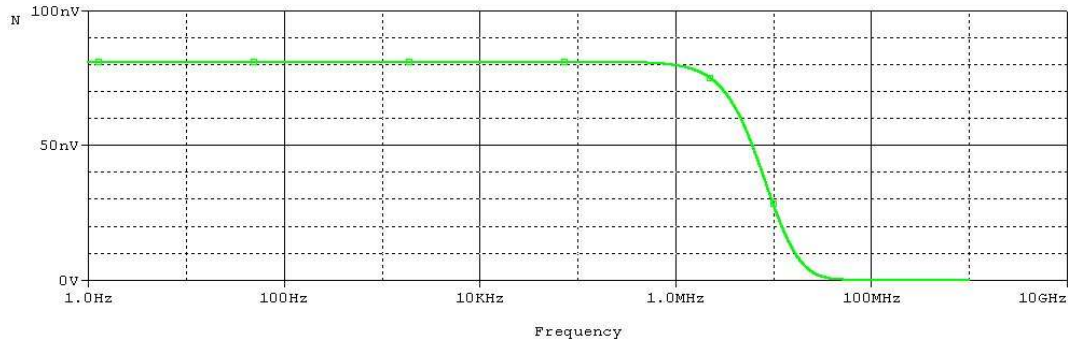


Figure 4.18 – Output-referred voltage spectral density of  $i_{R7}$  noise source  $N(f)$  [V/ $\sqrt{\text{Hz}}$ ]

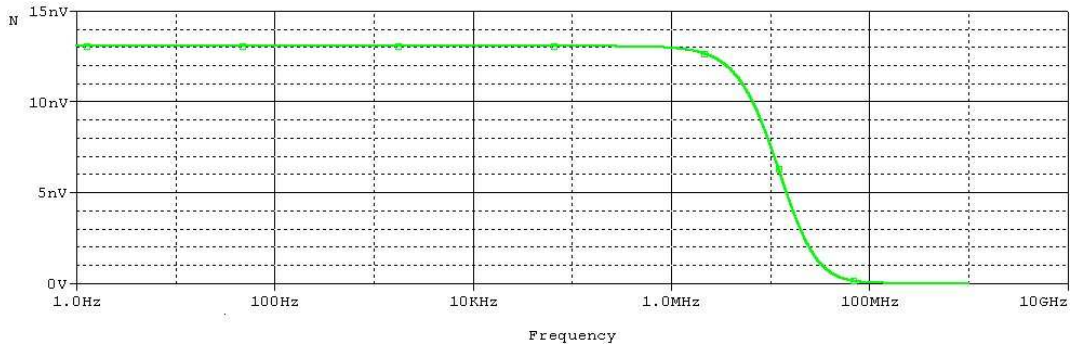


Figure 4.19 – Output-referred voltage spectral density of  $e_{N2}$  noise source  $N(f)$  [V/ $\sqrt{\text{Hz}}$ ]

We can calculate output-referred noise RMS voltage  $E$  for each noise source according to a following formula [16]

$$E = \sqrt{\int_0^{\infty} N(f)^2 df}, \quad (4.19)$$

where  $N(f)$  is an output-referred voltage spectral density. The following table shows the voltage and current input-referred noise spectral densities and the corresponding output-referred noise voltages.

Noise source	Voltage/Current spectral density	Output-referred RMS voltage noise	
$i_{R1}$	1.07 pA/ $\sqrt{\text{Hz}}$	$E_{iR1}$	336 $\mu\text{V}$
$i_{R7}$	0.62 pA/ $\sqrt{\text{Hz}}$	$E_{iR7}$	195 $\mu\text{V}$
$i_N$	1.20 pA/ $\sqrt{\text{Hz}}$	$E_{iN}$	376 $\mu\text{V}$
$e_{N1}$	1.30 nV/ $\sqrt{\text{Hz}}$	$E_{eN1}$	165 $\mu\text{V}$
$e_{N2}$	1.30 nV/ $\sqrt{\text{Hz}}$	$E_{eN2}$	39 $\mu\text{V}$

Table 1 – Input-referred noise sources and corresponding output-referred noise voltages

The total output noise voltage can be calculated as a square root of a sum of the noise voltage squares

$$E_{TOT} = \sqrt{E_{iR1}^2 + E_{iR7}^2 + E_{iN}^2 + E_{eN1}^2 + E_{eN2}^2}. \quad (4.20)$$

The total output-referred RMS voltage noise added by the amplifier is  $E_{TOT} = 570 \mu\text{V}$  RMS. It conforms to 4.38 nA of input-referred equivalent noise current ( $ENC$ ). According to equation 3.3 the  $ENC$  can be expressed by the charge of electron ( $e^-$ ) and amplification  $g_q$ :  $ENC = 14.6 e^-$  for  $g_q = 300 \text{ pA}/e^-$  or  $ENC = 7.3 e^-$  for  $g_q = 600 \text{ pA}/e^-$ . We can calculate signal to noise ratio  $SNR$  according the equation

$$SNR = 20 \log \left( \frac{I_S}{I_N} \right), \quad (4.21)$$

where  $I_N$  is the input referred noise current and  $I_S$  is a full scale input signal. If the estimated noise current  $I_N = 4.38 \text{ nA}$  and the full scale input signal is  $I_S = 30 \mu\text{A}$  than  $SNR = 76 \text{ dB}$ .

## 4.6 Subtracting Voltage Regulation

The subtracting voltage represented by  $V_I$  voltage source in Figure 4.8 can be digitally configured. Changing the subtracting voltage affect the pedestal current, and proportionally the gain of the DEPFET pixel. The subtracting voltage can be

simply set via a 3-wire SPI interface for each readout channel with 10-bit resolution. Figure 4.20 shows a block diagram of an octal DAC AD5318 described in [20] that is used for the subtracting voltage trimming.

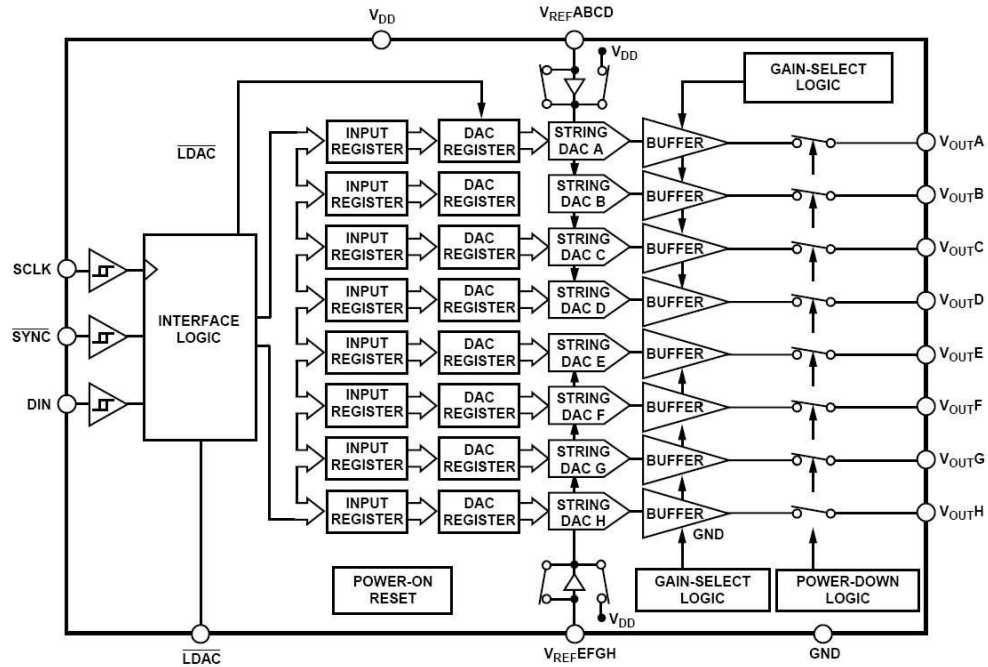


Figure 4.20 – The Octal DAC Block Diagram [20]

The output buffer amplifiers of each DAC provide rail-to-rail output swing. A slew rate of each output buffer is  $0.7 \text{ V}/\mu\text{s}$ . DAC A, DAC B, DAC C, and DAC D share a common reference input,  $V_{REFABCD}$ . DAC E, DAC F, DAC G, and DAC H share a common reference input,  $V_{REFEFGH}$ . Each reference input can be buffered, or can be unbuffered to give a reference input range from 0.25 V to the supply voltage, or can come from the supply voltage. The device has a power-down mode in which all DACs can be turned off individually with a high impedance output.

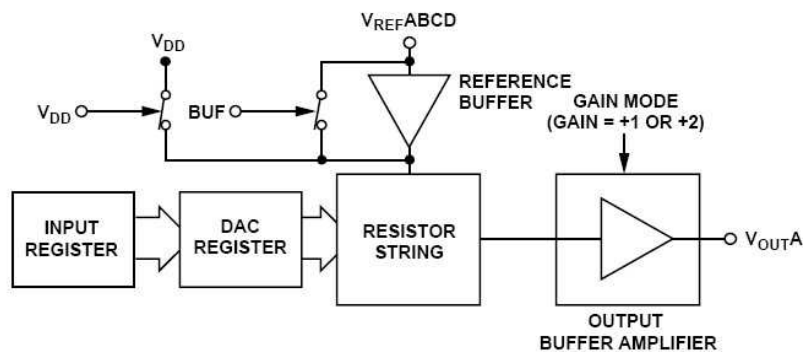


Figure 4.21 – The One DAC Channel Block Diagram [20]

The architecture of one DAC channel consists of a resistor string DAC that is followed by an output buffer amplifier. The voltage  $V_{REF}$  is the reference voltage for the corresponding DAC. Figure 4.12 shows a block diagram of the DAC one channel. The input coding to the DAC is binary, so the ideal output voltage  $V_{OUT}$  is given by [20]

$$V_{OUT} = \frac{V_{REF} D}{2^N}, \quad (4.22)$$

where  $D$  is the decimal equivalent of the binary code that is loaded to the DAC register (0 ÷ 1023), and  $N$  is the DAC resolution (10 bits).

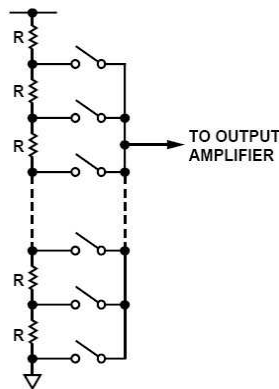


Figure 4.22 – The Resistor Net [20]

The resistor-string function is shown in Figure 4.22. It is simply a string of resistors, each of value  $R$ . The digital code is loaded to the DAC register and determines at which node on the string the voltage is tapped off. The output voltage goes then into the output amplifier. The voltage is tapped off by closing one of the switches connecting the string to the amplifier.

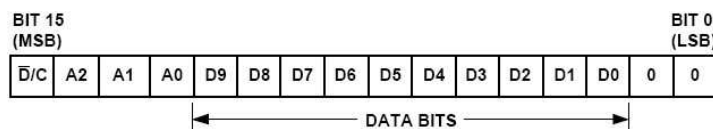


Figure 4.23 – The Input Shift Register Structure [20]

The 3-wire serial interface operates at clock rates up to 30 MHz and is compatible with SPI, QSPI, MICROWIRE, and DSP interface standards. The input shift register is 16 bits wide. Data is loaded into the device as a 16-bit word controlled by a serial clock input SCLK. The  $\overline{\text{SYNC}}$  input is a level-triggered input that acts as a frame synchronization signal and chip enable. Data can be transferred into the device only while  $\overline{\text{SYNC}}$  is low. To start the serial data transfer,  $\overline{\text{SYNC}}$  has to be low. After  $\overline{\text{SYNC}}$  goes low, serial data is shifted into the input of the device's shift register on the falling edges of SCLK for 16 clock pulses. To end the transfer,  $\overline{\text{SYNC}}$  must be taken high after the falling edge of the 16th SCLK pulse. After the end of the serial data transfer, data is automatically transferred from the input shift register to the input register of the selected DAC. If  $\overline{\text{SYNC}}$  is taken high before the 16th falling edge of SCLK, the data transfer is aborted and the DAC input registers are not updated.

The DACs are written and configured by writing into an input shift register. A structure of the register is shown in Figure 4.23. A MSB bit ( $\overline{\text{D/C}}$ ) is a control bit, determines if the DAC is written or configured. A2, A1, and A0 are address bits, determine which DAC is written or configured, and D9 ÷ D0 are data bits. Last two bits are unused. The DACs' output buffers are able to provide few mA output current that is enough for subtracting current. Because the subtracting voltage will be set only in the beginning of the measurement, low setting time is not required. It allows decoupling the output voltage by a large capacitor.

## 4.7 Differential to single-ended converter

The data acquisition ADC card is equipped with single ended inputs however a distance between the PC and the rest of the system could be quite long and the system could work in electromagnetic noisy background, so differential transmission lines are almost necessary. This problem is solved by differential to single-ended converters that are placed as close as possible to the ADCs' inputs and allow using the differential transmission lines for long distance.

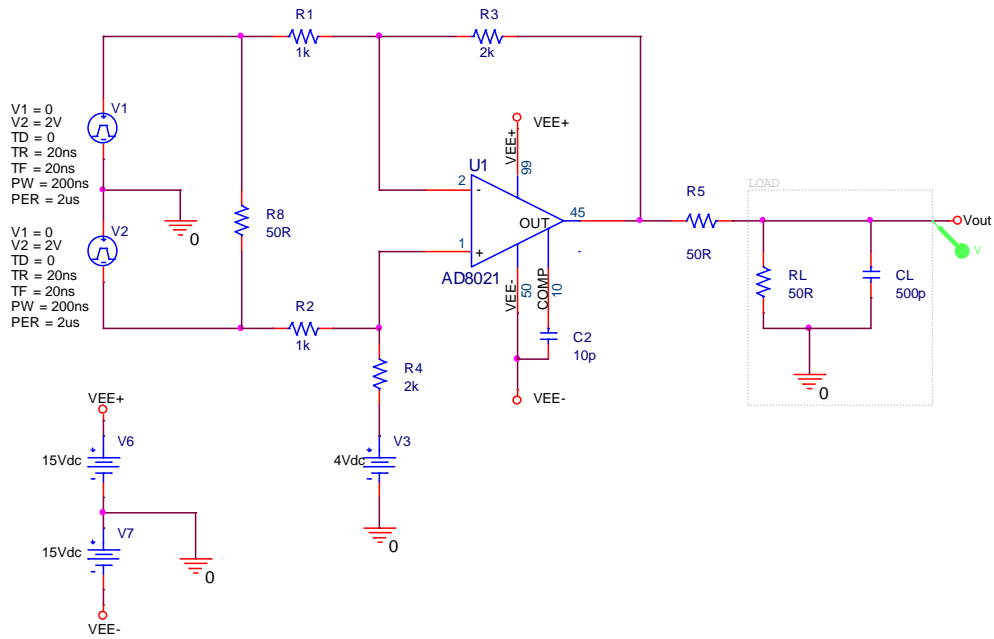


Figure 4.24 – Differential to Single-ended Converter

Figure 4.24 shows a schematic of the differential to single-ended converter. It contains a high speed low noise amplifier AD8021 described in [13]. It is able to deliver enough current to drive a  $50 \Omega$  line. We can calculate the output voltage  $V_{out}$

$$V_{out} = V_{in+} \left( \frac{R_3}{R_1} \right) + V_{in-} \left( -\frac{R_4}{R_2} \right) + V_3, \quad (4.23)$$

where  $V_{in+}$  and  $V_{in-}$  are positive and negative differential inputs,  $V_3$  is an offset voltage and  $R_3$ ,  $R_1$ ,  $R_4$  and  $R_2$  are corresponding resistances. Assuming that  $R_3/R_1 = R_4/R_2$ , formula 4.23 can be expressed

$$V_{out} = (V_{in+} - V_{in-}) \left( \frac{R_3}{R_1} \right) + V_3. \quad (4.24)$$

According to formula 4.24 this circuit takes the difference of the inputs, applies a scaling factor of  $R_3/R_1$  and adds an offset  $V_3$ . Resistors  $R_5$  and  $R_8$  match the input and output of the converter to the  $50 \Omega$  transmission lines. Resistor  $R_L$  and capacitor  $C_L$  represent input of the ADC card. For better performance the transmission line

between the converter and the ADC card is matched on the load and source side so as the transmission line between the readout amplifier and the converter. The impedance matching network creates a voltage divider with a dividing factor  $\frac{1}{2}$ . This is compensated by gain 2 of the amplifier. Figures 4.25 and 4.26 show results of a transient and an AC analysis. The cut-off frequency 10 MHz high enough and the output voltage levels corresponding to the ADC input.

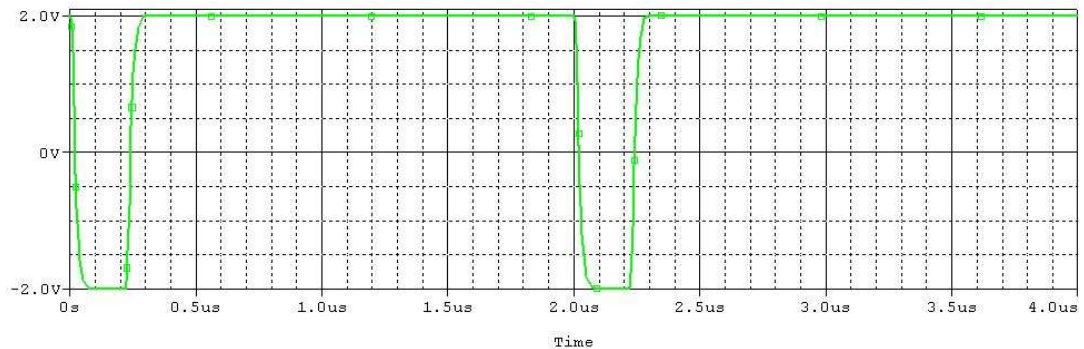


Figure 4.25 – Transient Analysis of the Differential to Single-ended Converter

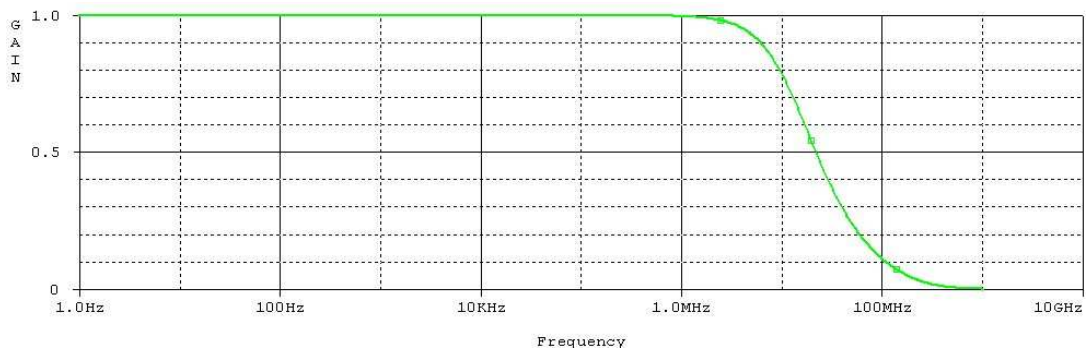


Figure 4.26 – AC Analysis of the Differential to Single-ended Converter

## 4.8 Switching Circuit

The switching circuit will drive DEPFET Mini-matrix Gates and Clear electrodes. It is analogous to the SWITCHER made of discrete components, but it's providing more flexible measuring. The DEPFET Mini-matrix requires 6 switches for the Gate electrodes and 6 switches for the Clear electrode. Together the

switching circuit contains 12 analog independent double-throw switches with 12 individual 3.3 V CMOS input logical control. To prevent interferences with the control X Board V2 with a FPGA the logical inputs contain galvanic separation.

#### Switching circuit requirements

- 12 independent double-throw switches
- Individual logical control input for each switch
- Precision timing of the switches with resolution of 5 ns
- Analogue voltage swing up to 15 V
- Switched voltage rising and falling time up to 50 ns
- Compatibility with the FPGA X Board V2

In Figure 4.27 is a functional diagram of a selected integrated circuit with switches ADG1434 described in [14]. It's the bidirectional double-throw quad switch with individual control of each switch. Typical on resistance of each switch is  $R_{on} = 6 \Omega$ . This circuit is very advantageous, because it's associating four individual switches in one package and it allows us to use only 3 integrated circuits to create all 12 switches.

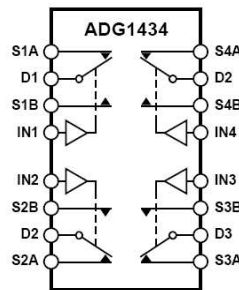


Figure 4.27 – Functional diagram of an ADG1434 quad analog switch [14]

Figure 4.28 shows a schematic of the one channel switch and simulated load circuit. Each channel consists of  $\frac{1}{4}$  of ADG1434 analogue switch (U1) and galvanic separator ADuM1100 (U2) that is insulating digital control inputs. The input side of the coupler is powered from an auxiliary power connector on the FPGA X Board V2 and has a separated ground. An additional RC filters are added to the logical inputs to cut-off noise frequencies. The load circuit simulates expected behaving of the DEPFET matrix and connecting wires.  $L_L$  represents an inductance of wires and a

ceramic socket. For estimated length of wire 5 cm and a backward wire 2 cm spacing  $L_L \approx 100$  nH.  $C_L$  is a DEPFET Gate or Clear electrode and wire capacity. Approximately,  $C_L \approx 10$  pF.  $R_L$  represent a leakage resistance  $R_L \approx 1$  M $\Omega$ .

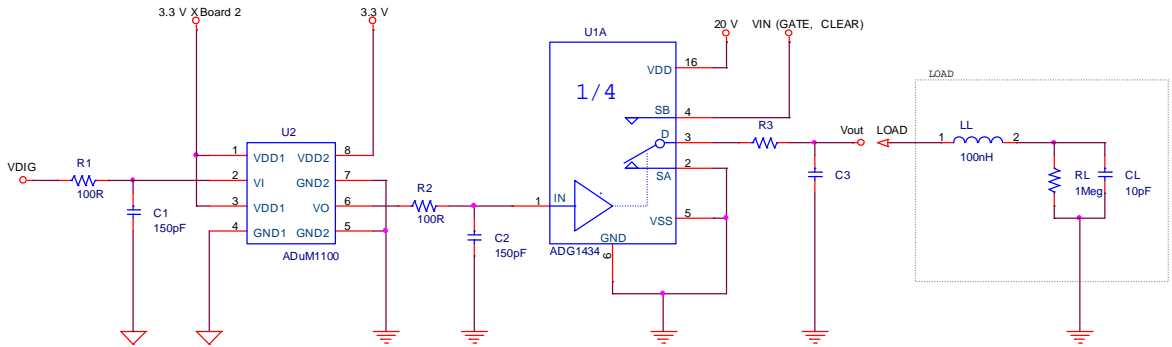


Figure 4.28 – Schematic of an one-channel switch and simulated load circuit

Figures 4.29, 4.30 and 4.31 show a PSpice simulation of the output voltage  $V_{out}$  response to the input digital signal  $V_{DIG}$  as a function of a load capacity  $C_L$ , an analog input voltage  $V_{IN}$  and temperature  $\nu$ . Simulated turn on time is  $t_{ON} = 120$  ns and turn off is  $t_{OFF} = 98$  ns for conditions  $C_L = 10$  pF,  $V_{IN} = 10$  V and  $\nu = 27$  °C. Definitions of  $t_{ON}$  and  $t_{OFF}$  are shown in the figure 6.

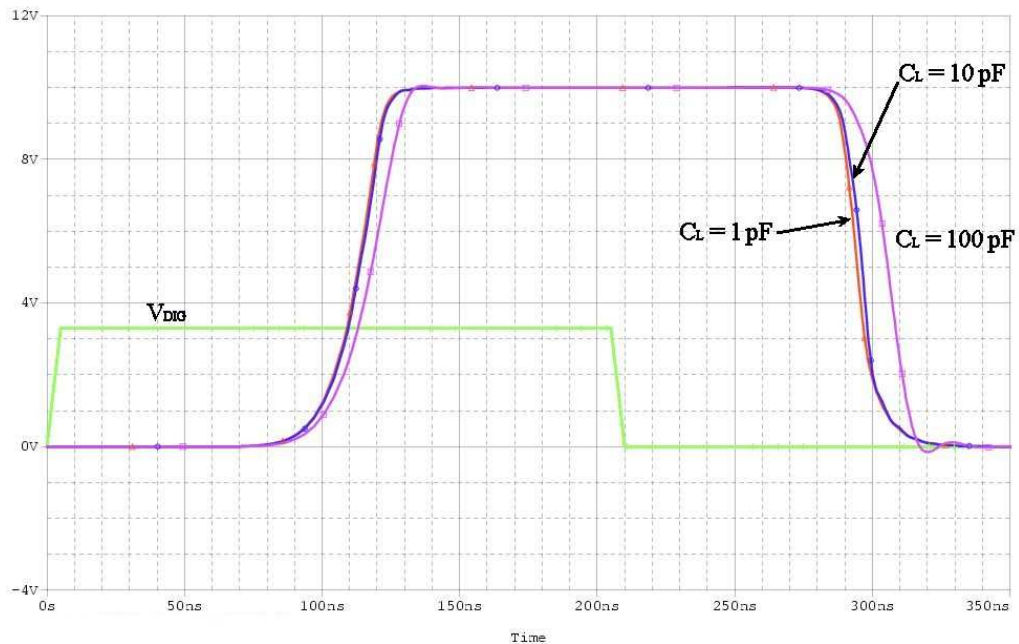


Figure 4.29 – Analog output voltage  $V_{out}$  response to the input digital signal  $V_{DIG}$  as a function of a load capacity  $C_L$  ( $V_{IN} = 10$  V,  $\nu = 27$  °C)

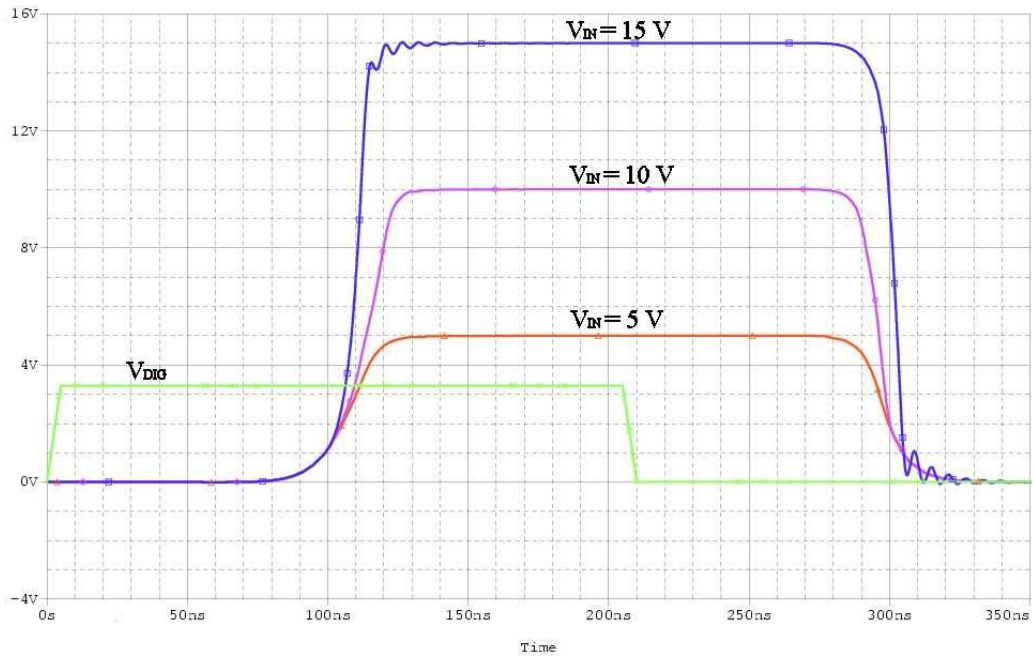


Figure 4.30 – Analog output voltage  $V_{out}$  response to the input digital signal  $V_{DIG}$  as a function of an analogue input voltage  $V_{IN}$  ( $C_L = 10$  pF,  $v = 27$  °C)

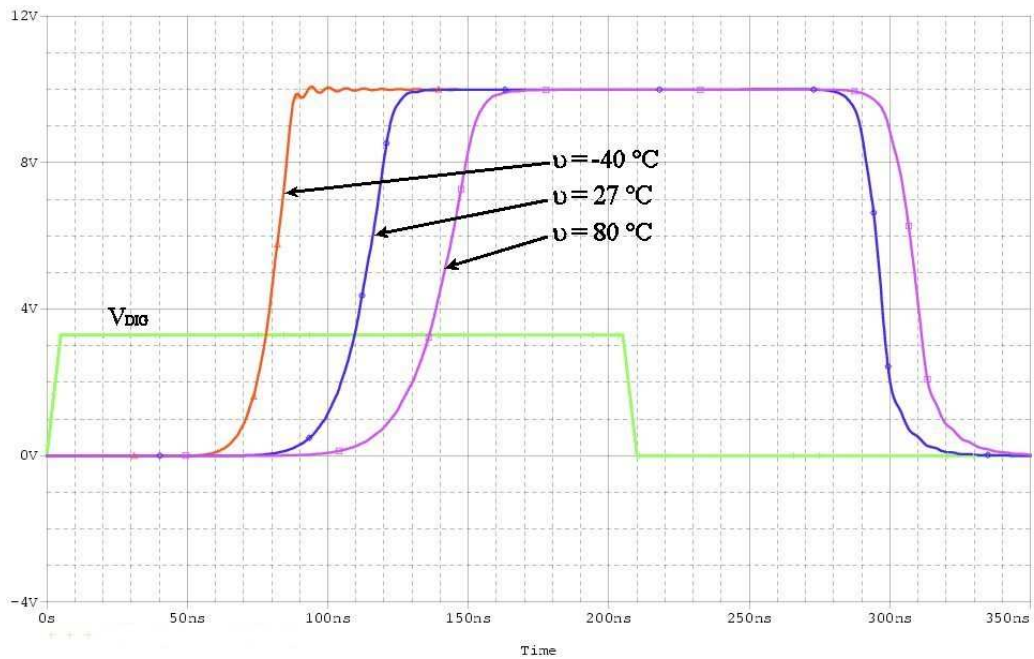


Figure 4.31 – Analog output voltage  $V_{out}$  response to the input digital signal  $V_{DIG}$  as a function of a temperature  $v$  ( $C_L = 10$  pF,  $V_{IN} = 10$  V)

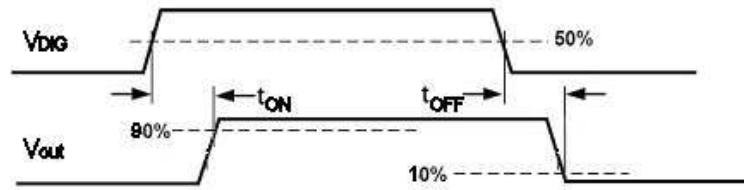


Figure 4.32 –  $t_{ON}$  and  $t_{OFF}$  definition

In Figure 4.33 is a functional block diagram of the ADuM1100 discussed in [21]. It is a digital isolator made by Analog Devices Inc. Combining high speed CMOS and monolithic air core transformer technology, this isolation component provides good performance characteristics for 3.3 V CMOS logic superior to alternatives, such as optocoupler devices. This digital isolator insert in the input digital signal an additional propagation delay approximately 15 ns at room temperature as shown in Figure 4.34.

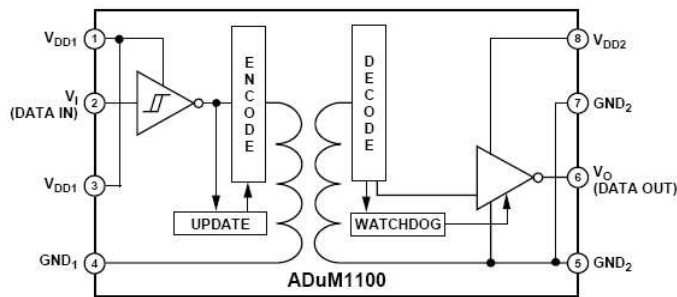


Figure 4.33 – Functional block diagram of a galvanic separator ADuM1100 [21]

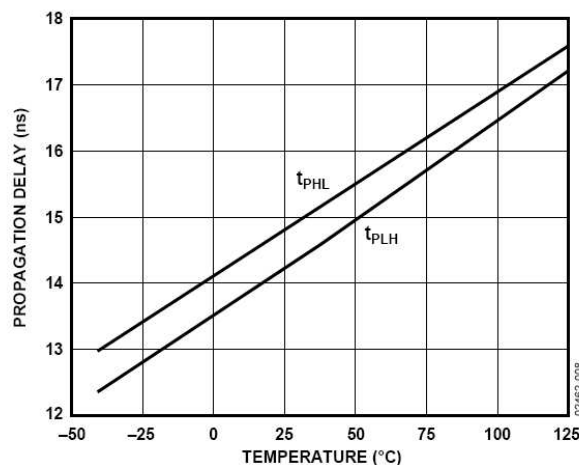
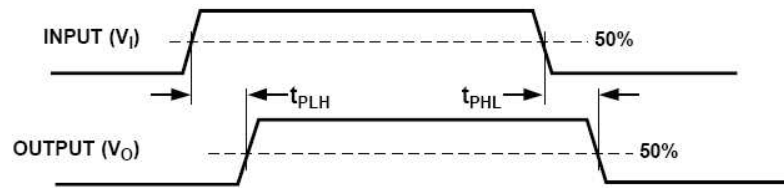


Figure 4.34 – Propagation delay as a function of temperature of a galvanic separator ADuM1100 (Datasheet plot) [21]

Figure 4.35 – Definitions of  $t_{PLH}$  and  $t_{PHL}$ 

The circuit described above should satisfy the requirements as the wide output voltage swing, and the various load capacities. As shown in Figures 4.29, 4.30 and 4.31 the turn on delay  $t_{ON}$  and turn off delay  $t_{OFF}$  are dependent of temperature  $\mathcal{V}$ , load capacity  $C_L$ , and input analogue voltage  $V_{IN}$ . Also changes of these parameters cause a different output pulse length distortion. The temperature drift affect also digital separator as shown in Figure 4.34. It could be difficult to predict exact output pulse position in range of 5 ns, but calibration and direct measuring will be possible.

# Chapter 5

## Conclusions

The measuring system described in the thesis was designed for the DEPFET Mini-matrices with 16 x 6 pixels. The new measurements on the DEPFET Mini-matrix require almost completely new measuring system. The designed system allows to measure charge stored in each pixel with the dynamical range about 70 dB. It will be very interesting to study processes as charge sharing among multiple pixels. Also measurement the charge loss from the internal gate of the DEPFET will be important. The multi-pixel structure readout in addition to the single pixel readout will help to understand where the charge is loosing to. Another advanced function that is provided by the new measuring system is an autonomous control of each Clear and Gate DEPFET matrix terminals. This function allows studying control signals timing and its influence on DEPFET matrix behaviour. Especially Gate signals timing have strong impact on dynamic parameters of the readout electronics. When the next row is selected during the DEPFET matrix readout by switching the Gate voltages, it cause a high drain current swing, if there is a delay between the previous and following gate signals. This high drain current swing, which has negative affect on the readout electronics could be eliminated by the Gate signals overlapping.

The designed system is associating a commercial electronics, control electronics that was designed in the Max-Planck institute earlier and a new readout and steering electronics that has not been produces yet. The system contains four main blocks. The PC with the 8-channel 14-bit 100 Msps PCI data acquisition card, X Board V2 FPGA control card, the current readout and switching circuit and the differential to single-ended converter. The data acquisition ADC card is the commercial PC card OCT-838-007. The signal to noise ratio  $SNR_{ADC}$  of the data acquisition card is 68 dB and the effective number of bits of the ADC  $ENOB$  is 11 bits. The effective number of bits will be increased by additional software operations as averaging. The X

Board v2 is the FPGA card that was made in the Max-Planck Institute in Munich. The X Board providing communication with the PC via the USB port. The board is also clocking and the triggering the ADCs, and providing digital signals for the switching circuit and current readout amplifiers setting.

The DEPFET drain current readout circuit is placed together with the switching circuit on the same PCB. It's made of 8 drain readout amplifiers and the switching circuit contains 12 individual analog switches that control the Gate and Clear electrodes of the DEPFET Mini-matrix sensor. The parameters of the current readout electronics were simulated and the results from the single pixel readout setup were taken into account. The total output-referred RMS voltage noise of the drain readout amplifier  $E_{TOT}$  is 570  $\mu\text{V}$  RMS that is equivalent to 4.38 nA of input-referred noise current. Equivalent noise  $ENC$  is 14.6  $e^-$  for  $g_q = 300 \text{ pA}/e^-$  or 7.3  $e^-$  for  $g_q = 600 \text{ pA}/e^-$ . The signal to noise ratio of the readout amplifier  $SNR$  is 76 dB. Simulated turn-on time of the switching circuit is  $t_{ON} = 120 \text{ ns}$  and the simulated turn-off time is  $t_{OFF} = 98 \text{ ns}$  for the standard conditions, load capacity 10 pF, input voltage 10 V, and temperature 27  $^\circ\text{C}$ .

The designed system should satisfy all measurements that are necessary to do at the DEPFET Mini-matrices. It's flexible and it allows doing additional upgrades and modifications. Expected total cost is approximately 12,000 EUR.

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